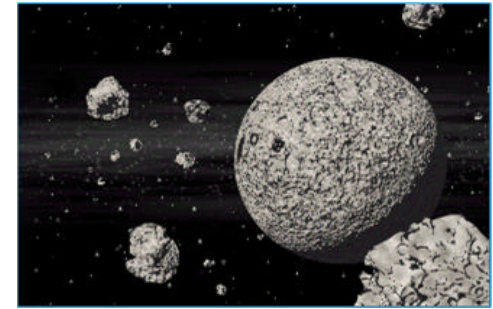


Asteroid-Z

MS-7423N1

Version 0B



CPU:

YorkField, Wolfdate, Conroe, Conroe-1M,
Conroe-L ; TDP max=65W, FSB 1333/1066/800

System Chipset:

Intel Q45 (North Bridge)
Intel ICH10DO (South Bridge)

On Board Chipset:

BIOS -- SPI FLASH 32MB
HD AUDIO Codec -- ALC262
LPC Super I/O -- SMSC SCH5617
LAN --INTEL 82567LM Boazman
Clock GEN-IDTCV184-2
TPM - SLB9635 TT1.2
PCMCIA - Ricon 5C812/PCI

Expansion Slots:

Half mini PCIE SLOT * 1

Main Memory:

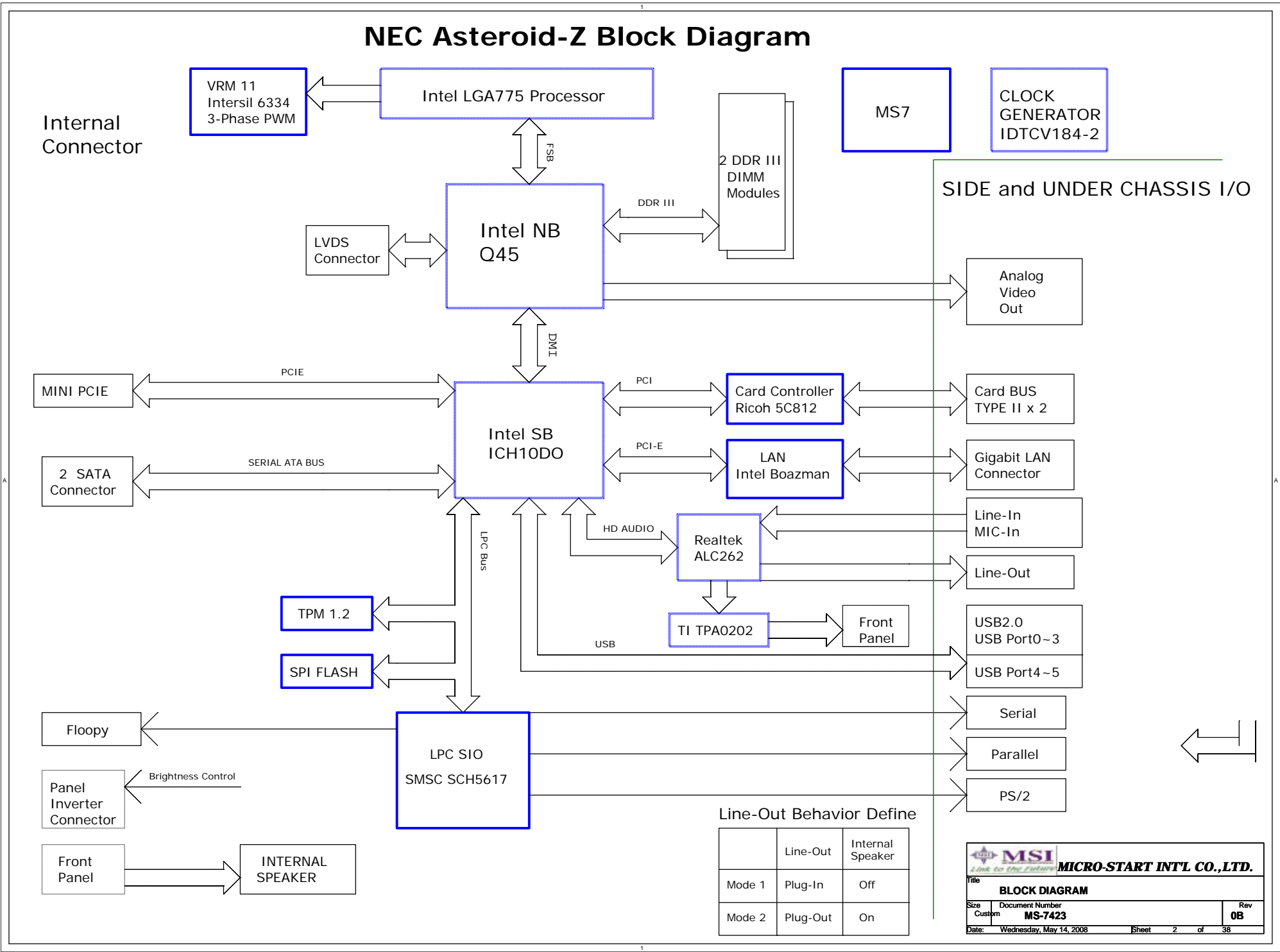
DDR III * 2 - 1066 w/o ECC

Intersil PWM:

Controller: Intersil 6334 3Phase


COVER SHEET	1
BLOCK DIAGRAM	2
Intel LGA775-CPU	3~5
CLOCK Generator-IDTCV184-2	6
Eaglelake-Q	7~11
DDR3 DIMM 1 & 2	12
CH7308 - LVDS Interface	13
ICH10	14~16
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GPIO MAP	33
POWER MAP	34
POWEROK MAP	35
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NEC Asteroid-Z Block Diagram



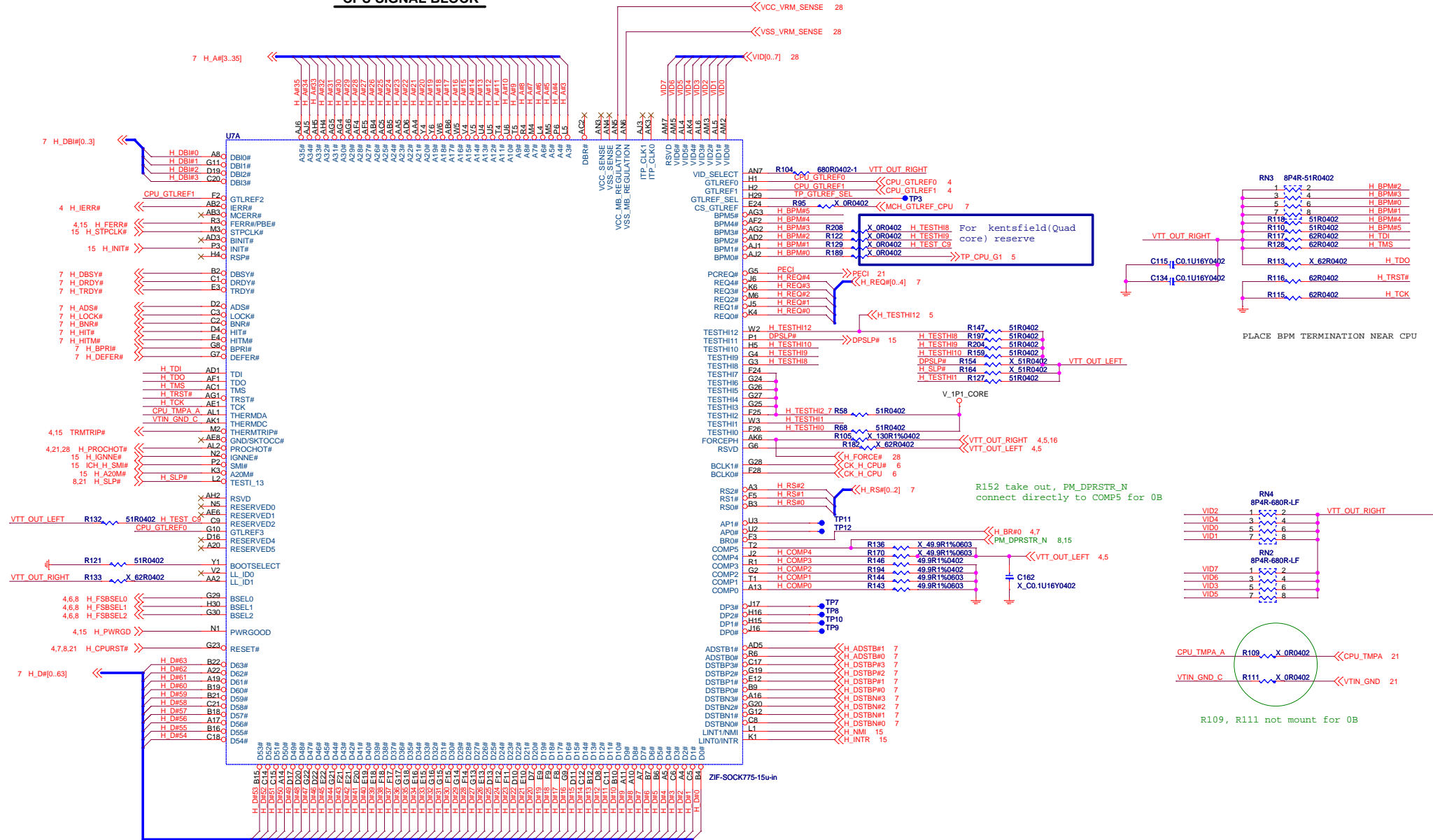
Line-Out Behavior Define

	Line-Out	Internal Speaker
Mode 1	Plug-In	Off
Mode 2	Plug-Out	On

**MICRO-START INT'L CO.,LTD.**

BLOCK DIAGRAM

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Custom	MS-7423	0B
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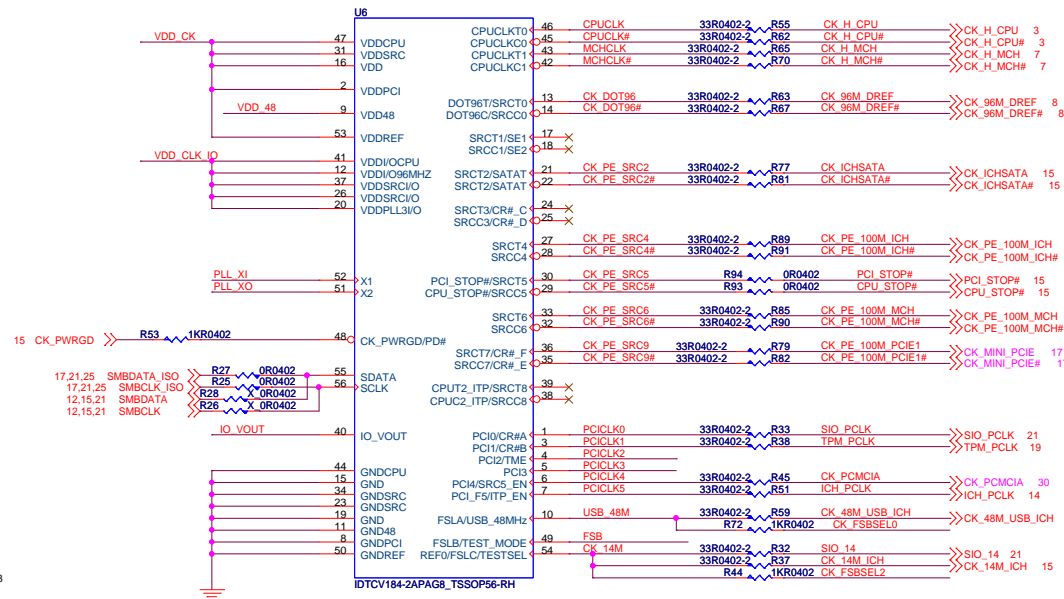


BSEL			TABLE
2	1	0	FSB FREQUENCY
0	0	0	267 MHZ (1067)
0	1	0	200 MHZ (800)
0	0	1	133 MHZ (533)
1	0	0	333 MHZ (1333)

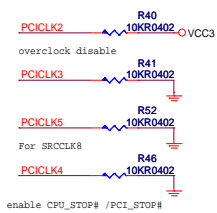
~~CLOCK Generator -~~ IDTCV184-2

VDD_CK Decoupling

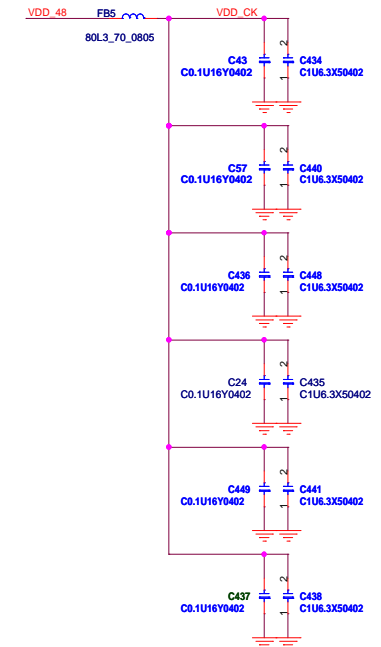
Place near each VDD_CK Pins



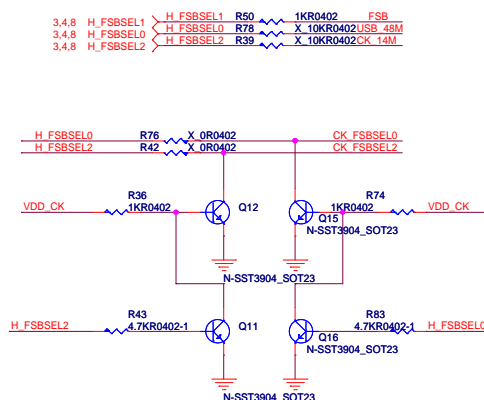
Strapping resistor



C28, C29 are changed from 27pF to 47pF for 0B

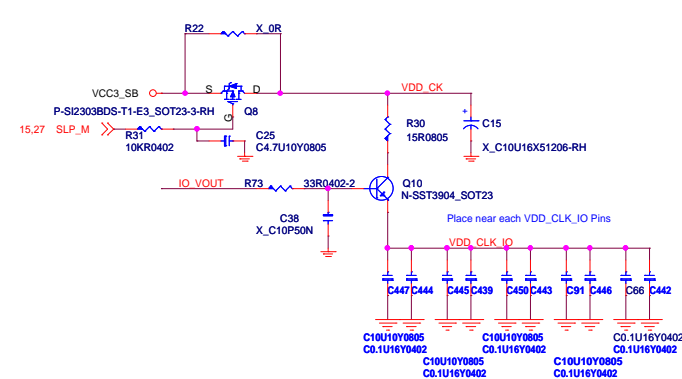


CPU Frequency select

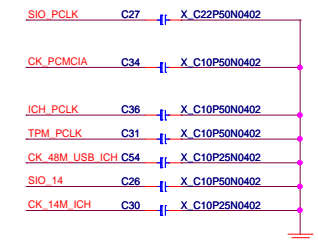


FS ₀ C ¹ 80b7	FS ₀ B ¹ 80b6	FS ₀ A ² 80b5	CPU MHz
0	0	0	255.66
0	0	1	133.33
0	1	0	200.00
0	1	1	166.66
1	0	0	333.33
1	0	1	100.00
1	1	0	400.00
1	1	1	Reserve

VDD_CK & VDD_CLK_IO Power



For EMI
reserver



MICRO-START INT'L CO., LTD.

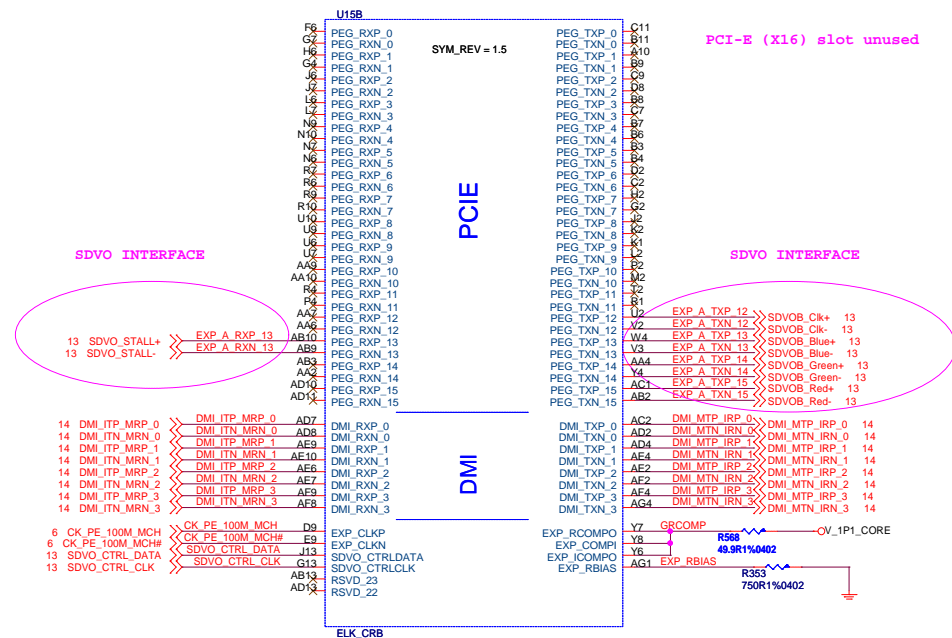
Title _____

CLOCK Generator-IDTCV184-2APAG8

MS-7423

Rev
0B

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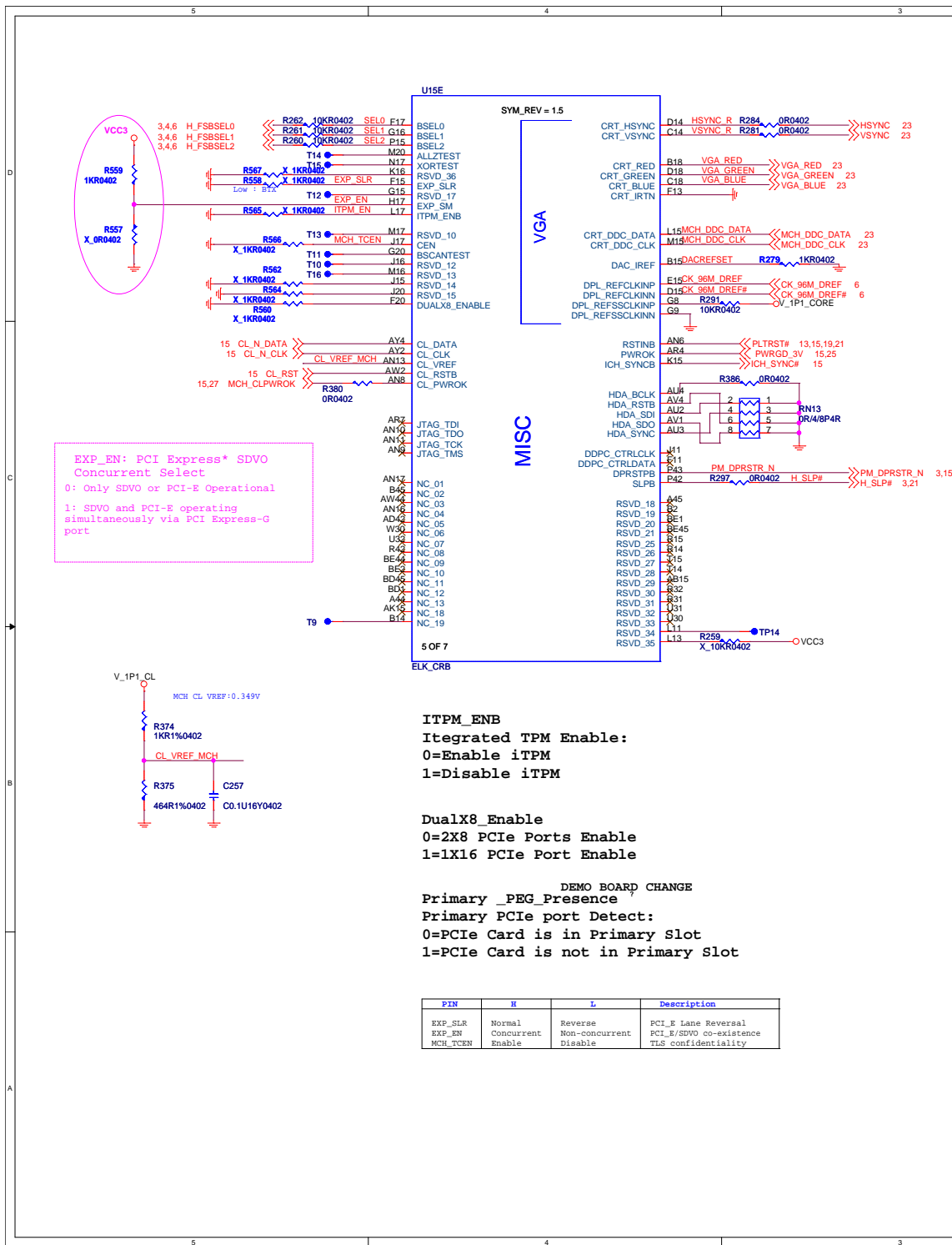
V1P1_CORE

C452 C0.1U16Y0402

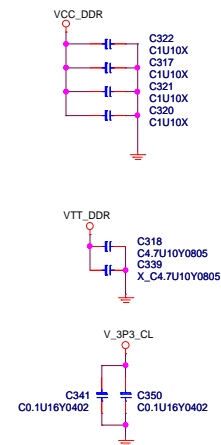
C199

C253 C0.1U16Y0402

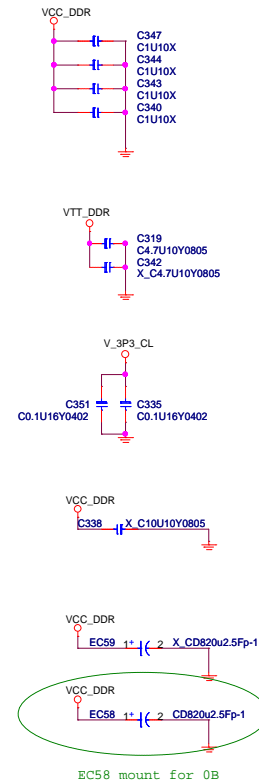
C0.1U16Y0402



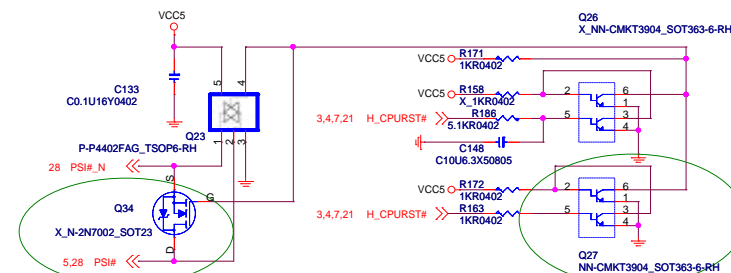
DIMM1 decoupling cap



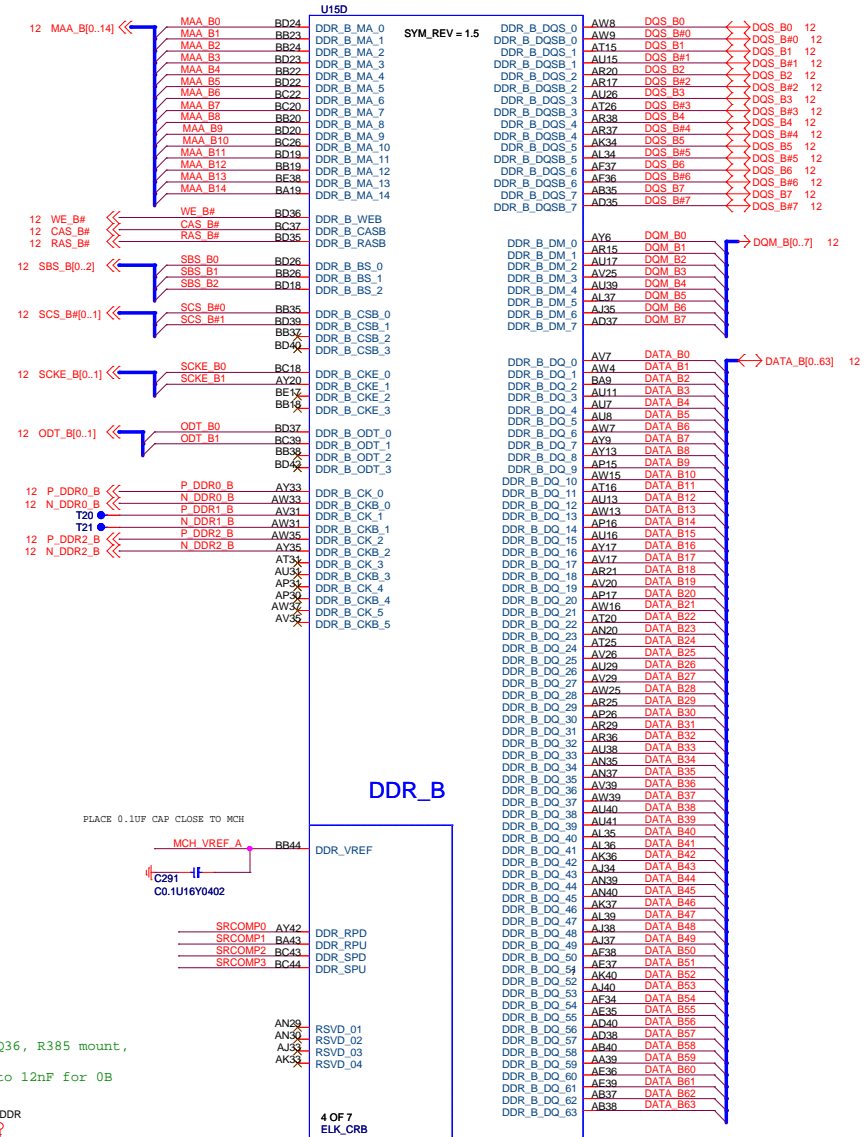
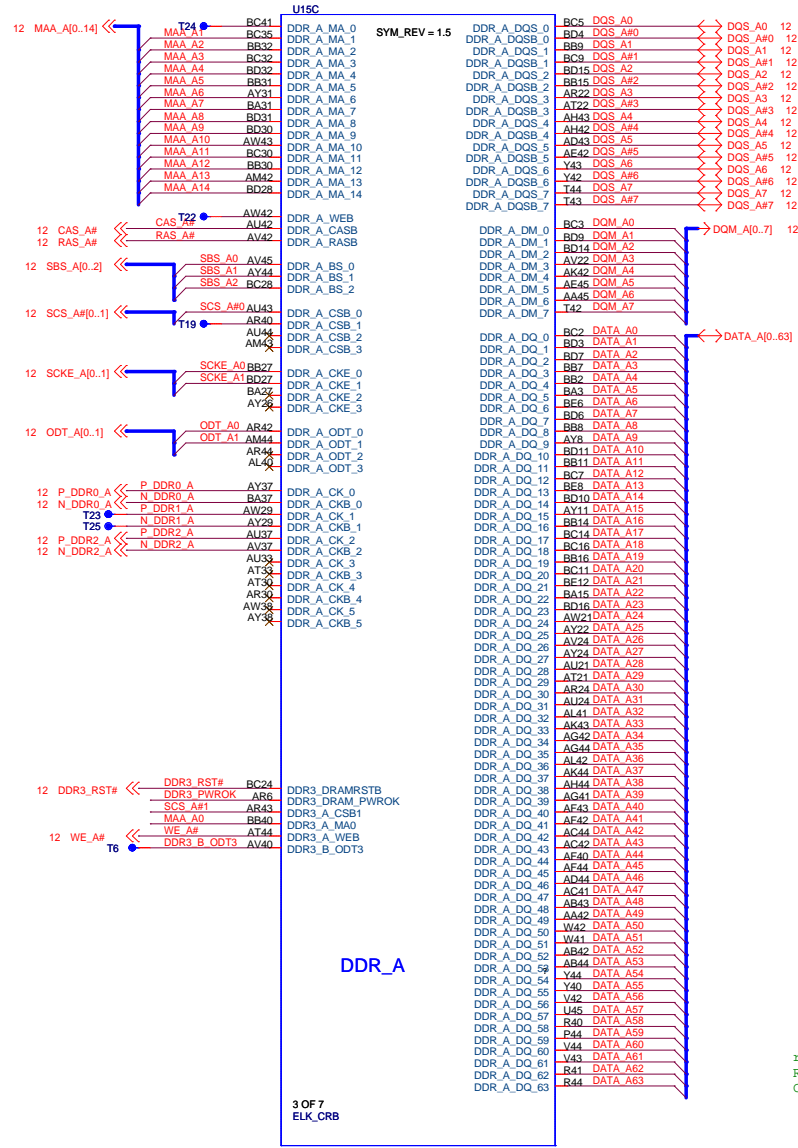
DIMM2 decoupling cap



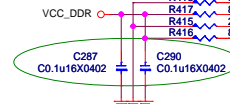
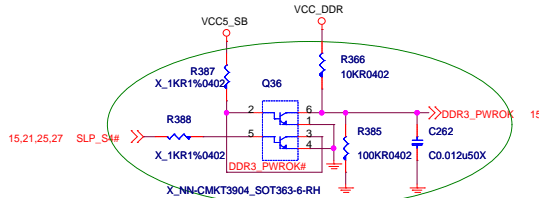
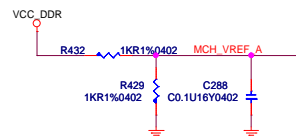
PSI (POWER STATE INDICATOR)



R158 no mount, Q27 mount, remove R142, add Q34 for 0B



remove Q54, Q56, add Q36, R385 mount,
R387& R388 not mount
C262 change from 1uF to 12nF for 0B



C287 change from Y5V to X7R;
C290 change from 0603 type/Y5V to 0402 type/X7R for 0B

MSI
MICRO-START INT'L CO.,LTD.

Eaglelake Memory

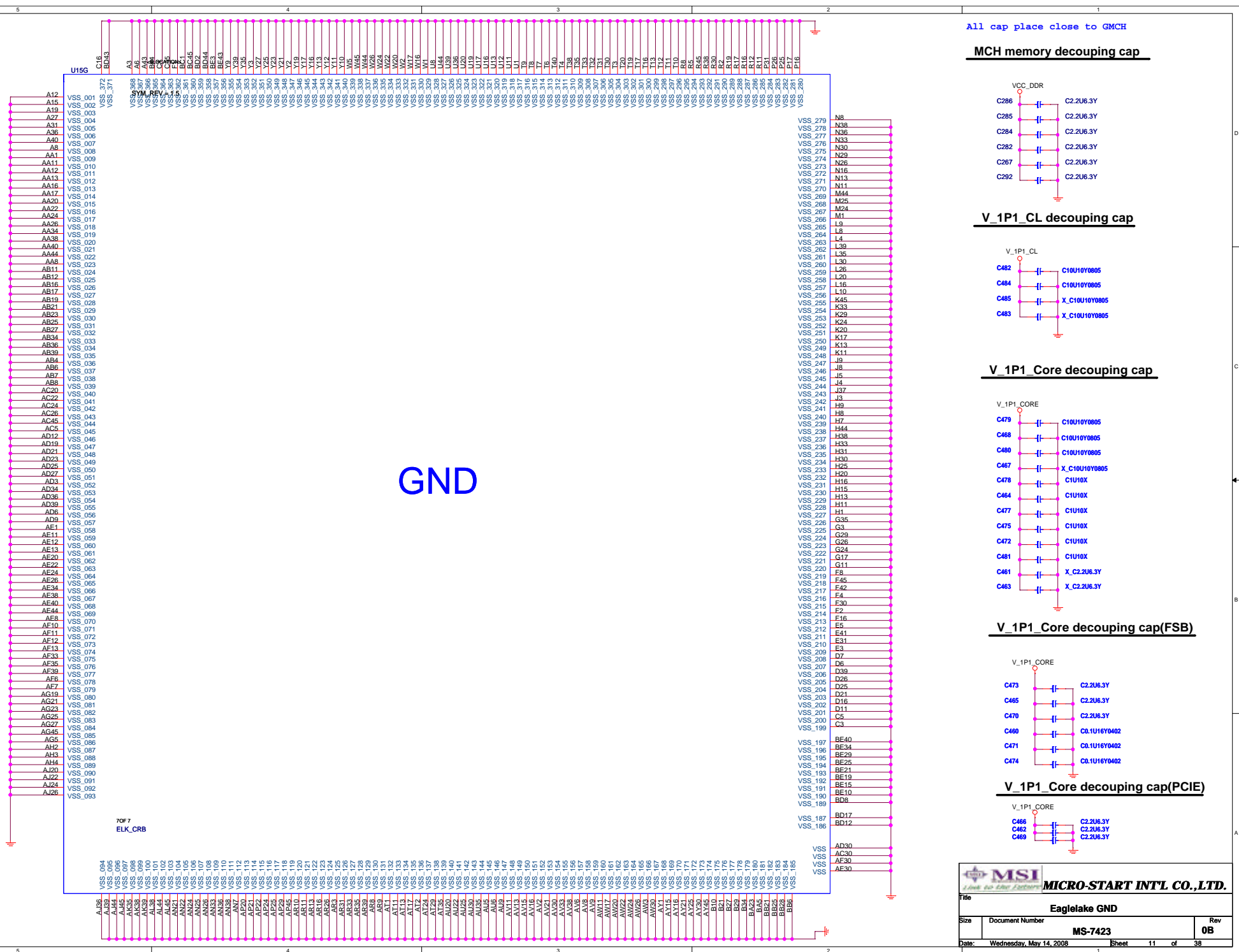
MS-7423

0B

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All cap place close to GMCH

MCH memory decoupling cap

VCC_DDR

C286 C2.2u6.3Y

C285 C2.2u6.3Y

C284 C2.2u6.3Y

C282 C2.2u6.3Y

C287 C2.2u6.3Y

C292 C2.2u6.3Y

V_1P1_CL decoupling cap

V_1P1_CL

C482 C10U10Y0805

C484 C10U10Y0805

C485 X_C10U10Y0805

C483 X_C10U10Y0805

V_1P1_Core decoupling cap

V_1P1_CORE

C479 C10U10Y0805

C468 C10U10Y0805

C480 C10U10Y0805

C467 X_C10U10Y0805

C478 C1U10X

C464 C1U10X

C477 C1U10X

C475 C1U10X

C472 C1U10X

C481 C1U10X

C461 X_C2.2u6.3Y

C463 X_C2.2u6.3Y

V_1P1_Core decoupling cap(FSB)

V_1P1_CORE

C473 C2.2u6.3Y

C465 C2.2u6.3Y

C470 C2.2u6.3Y

C460 C0.1U16Y0402

C471 C0.1U16Y0402

C474 C0.1U16Y0402

V_1P1_Core decoupling cap(PCIe)

V_1P1_CORE

C466 C2.2u6.3Y

C462 C2.2u6.3Y

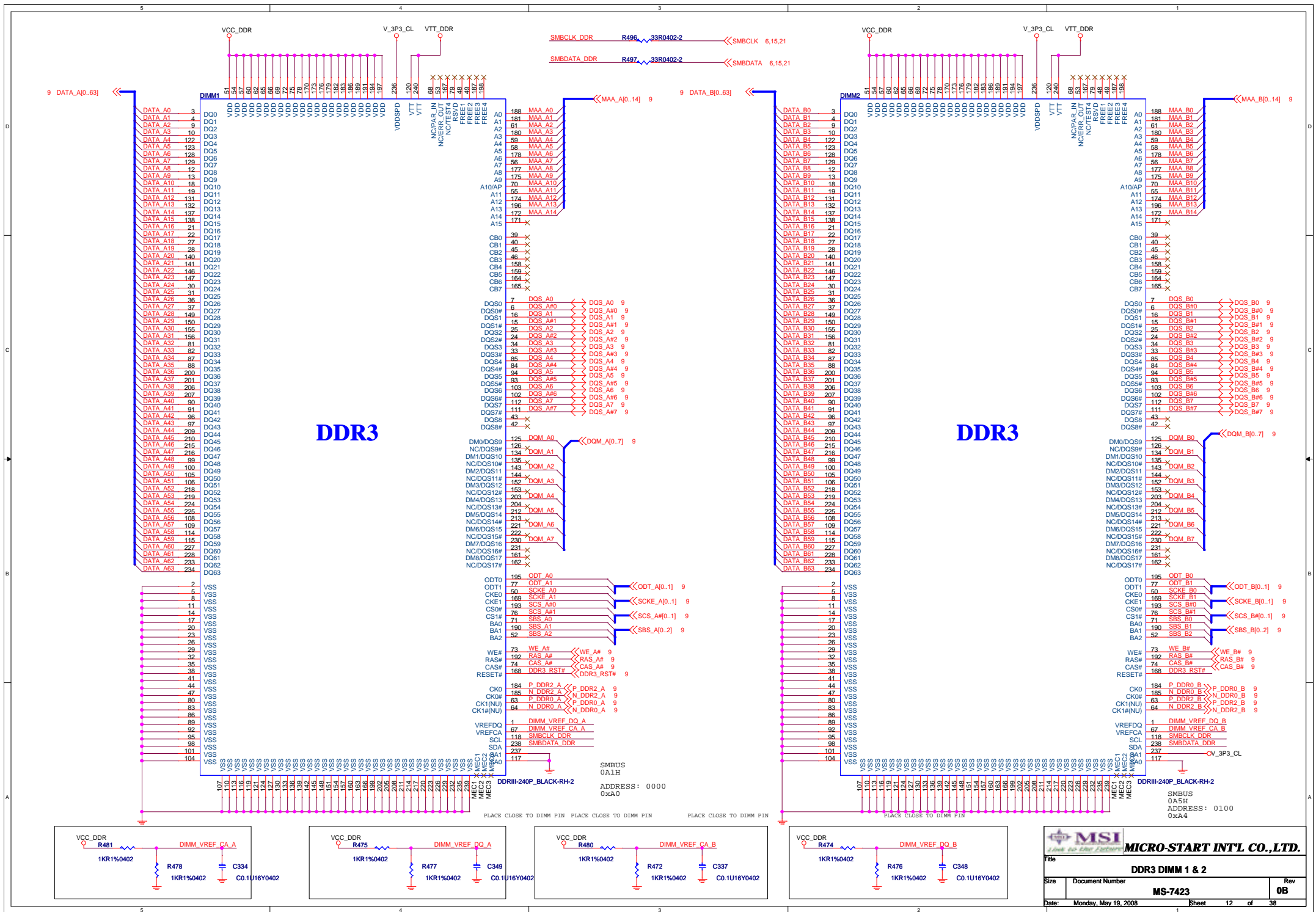
C469 C2.2u6.3Y

MICRO-START INT'L CO.,LTD.

File: Eaglelake GND

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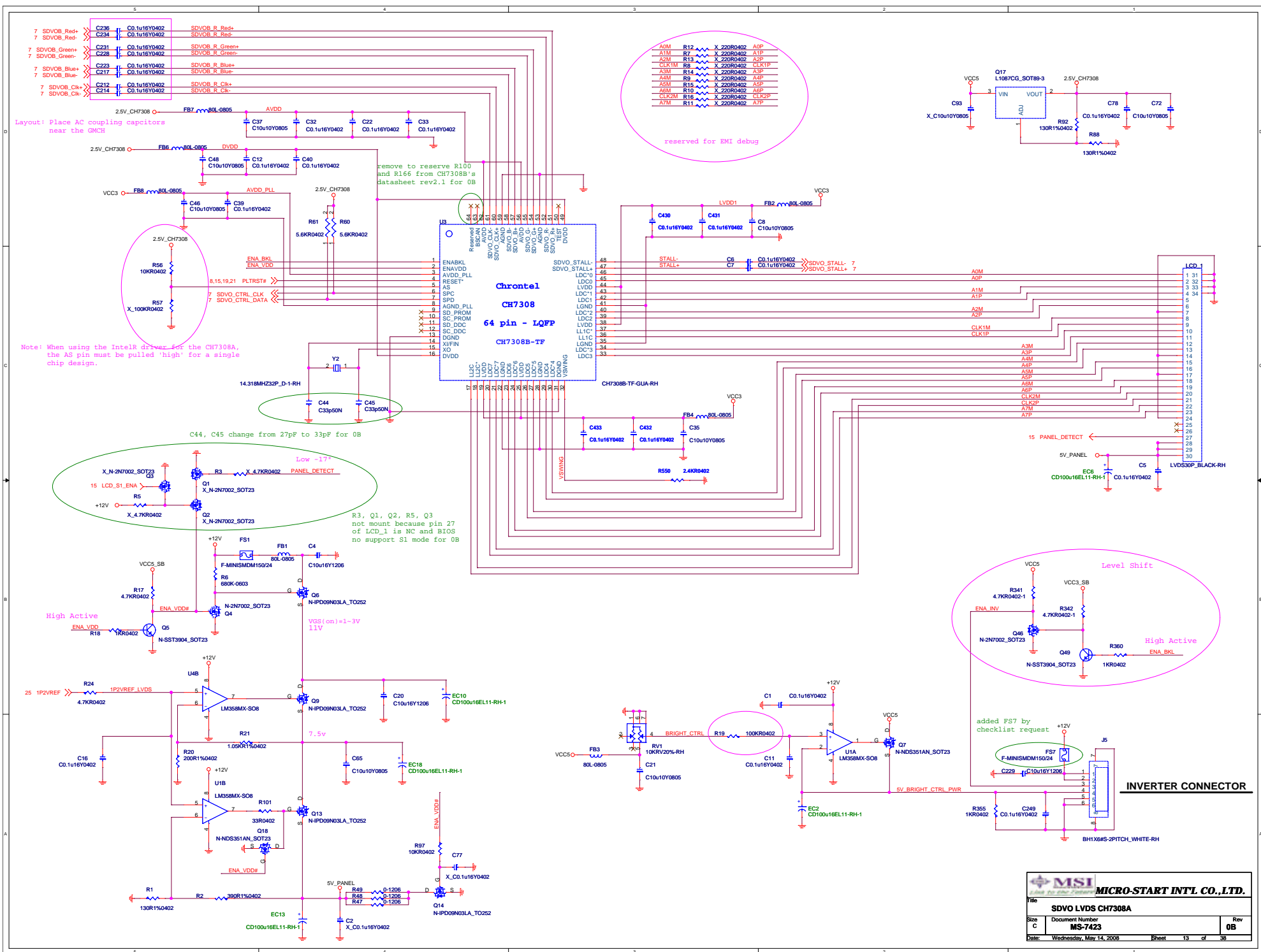
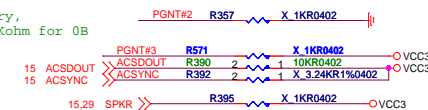


Figure 10 shows the PCI Express 1.1a pin connections for the 8P4R-2.7K0402-LF package. The package has 29 pins, with pins 1-4 and 5-8 being 0.5mm pitch headers, and pins 9-29 being 0.8mm pitch headers. The connections are as follows:

- Pin 1:** VCCS
- Pin 2:** PREQ#3
- Pin 3:** PCI_STOP#
- Pin 4:** PREQ#1
- Pin 5:** VCCS
- Pin 6:** 8.2K0402
- Pin 7:** R570
- Pin 8:** PREQ#2
- Pin 9:** VCCS
- Pin 10:** PCI_DEVSEL#
- Pin 11:** PCI_PERR#
- Pin 12:** LOCAL#
- Pin 13:** PCI_FRAME#
- Pin 14:** PCI_ERR#
- Pin 15:** VCCS
- Pin 16:** PCI_SERR#
- Pin 17:** PCI_IRDY#
- Pin 18:** PREQ#0
- Pin 19:** PCI_TRDY#
- Pin 20:** VCC3
- Pin 21:** PIROQA
- Pin 22:** PIROQC
- Pin 23:** PIROQB
- Pin 24:** PIROQD
- Pin 25:** VCC3
- Pin 26:** PIROQF
- Pin 27:** PIROQE
- Pin 28:** PIROQH
- Pin 29:** PIROQG



SIGNAL	H	L	DES.
SPKR	DIS	EN	REBOOT
GNT3	DIS	EN	A16 OVERIDE
INTVRMEN	EN	DIS	INT VRM
SATALED	NORM	REVERSE	PCIE 0-3 ORDER
HDA_SDOUT	DPX/ PCIE	N/A	XOR MODE/PCIE PORT CONFIG BIT 1
HDA_SYNC	SET BIT	N/A	PCIE PORT CONFIG BIT 0 (1-4)
GNT2	N/A	SET BIT	PCIE PORT CONFIG 2 BIT 0 (5-6)

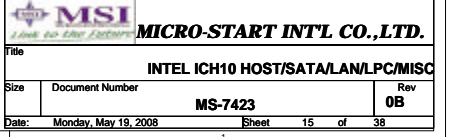
BOOT_DEVICE	GNT#0	SPI_CS1#	
FWH	1	1	
SPI	0	X	(Default)
PCI	1	0	



MS-7423

0B

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MINI PCI-E BLOCK

TP2
TP1

15 WAKE#

6 CK_MINI_PC1
6 CK_MINI_PC1

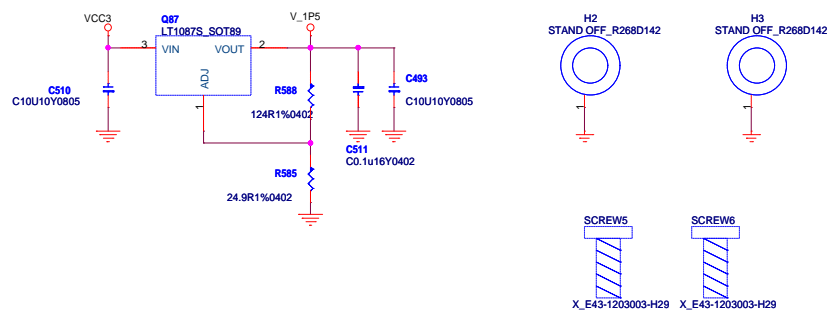
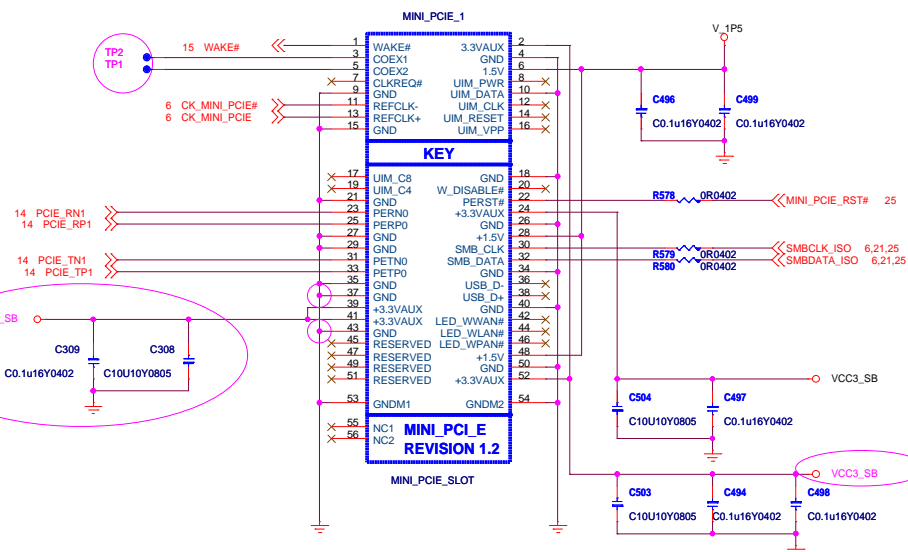
14 PCIE_RN1
14 PCIE_RP1

14 PCIE_TN1
14 PCIE_TP1

VCC3_SB

C309
C0.1u16Y0402

C308
C10U10Y0805



The diagram illustrates the SATA connections for the SATA7M and SATA7P components. The top section shows the SATA7M connections to the SATA7P_BLUE-P-RH component. The bottom section shows the SATA7P connections to the SATA7P_RED-P-RH component. A separate detail shows the J3 connector for the BH1X3B-FR_WHITE-RH component connected to VCC5.

SATA7M Connections:

- SATA_TX0 connects to C102, which is connected to C0.01U25X0402, which is connected to S_TX0.
- SATA_TX#0 connects to C108, which is connected to C0.01U25X0402, which is connected to S_TX#0.
- SATA_RX#0 connects to C107, which is connected to C0.01U25X0402, which is connected to S_RX#0.
- SATA_RX0 connects to C101, which is connected to C0.01U25X0402, which is connected to S_RX0.

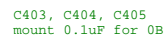
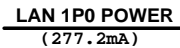
SATA7P Connections:

- SATA_TX1 connects to C106, which is connected to C0.01U25X0402, which is connected to S_TX1.
- SATA_TX#1 connects to C105, which is connected to C0.01U25X0402, which is connected to S_TX#1.
- SATA_RX#1 connects to C104, which is connected to C0.01U25X0402, which is connected to S_RX#1.
- SATA_RX1 connects to C103, which is connected to C0.01U25X0402, which is connected to S_RX1.

Connector Details:

- SATA7P_BLUE-P-RH:** 7-pin connector with pins 1 (GND), 2 (HT+), 3 (HT-), 4 (GND), 5 (HR-), 6 (HR+), and 7 (GND).
- SATA7P_RED-P-RH:** 7-pin connector with pins 1 (GND), 2 (HT+), 3 (HT-), 4 (GND), 5 (HR-), 6 (HR+), and 7 (GND).
- J3:** 5-pin connector with pins 1 (VCC5), 2 (GND), 3 (GND), 4 (GND), and 5 (GND).

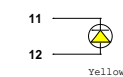
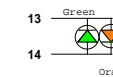
C381&C383 change from Y5V to X7R

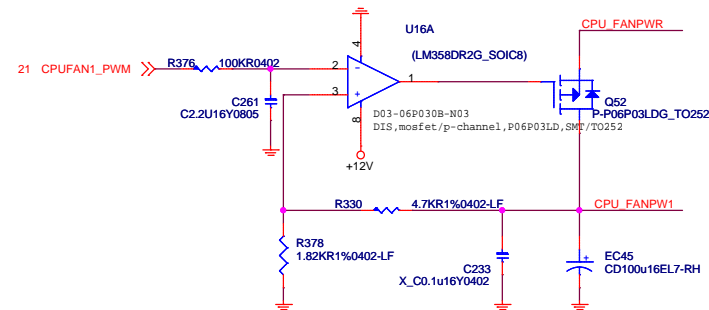
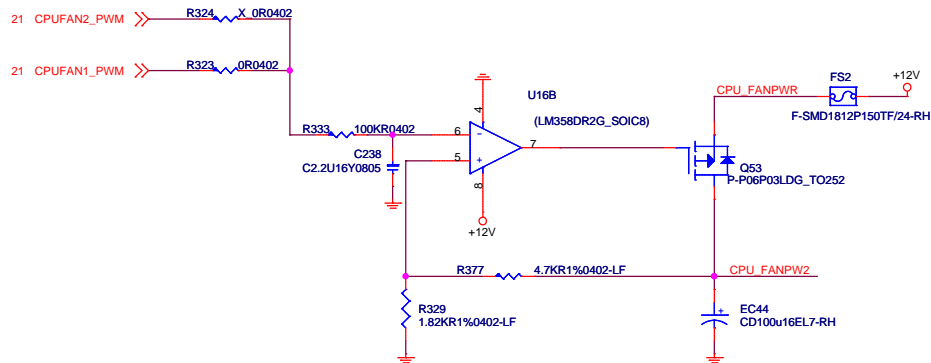
[illegible]

The schematic diagram illustrates the internal structure of a LAMC component. It features several input and output ports labeled 1 through 7. Key components include capacitors labeled \$C_{in}\$ and \$C_{out}\$, and resistors labeled \$R_{in}\$ and \$R_{out}\$. The circuit is connected to a common ground, indicated by a symbol at the bottom right. A label "LAMP" is present near the top left, and "GROUND" is labeled at the bottom right.

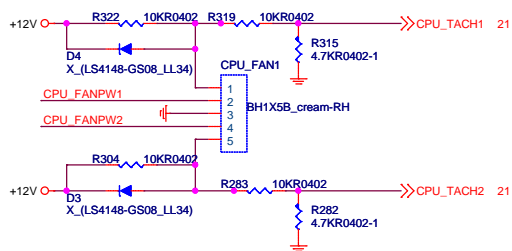
```
Speed LED Type
1000Mbps : Orange
100Mbps  : Green
10Mbps   : LED off
```

For Active/Link:
Yellow

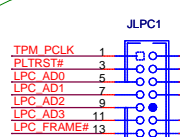




CPU FAN



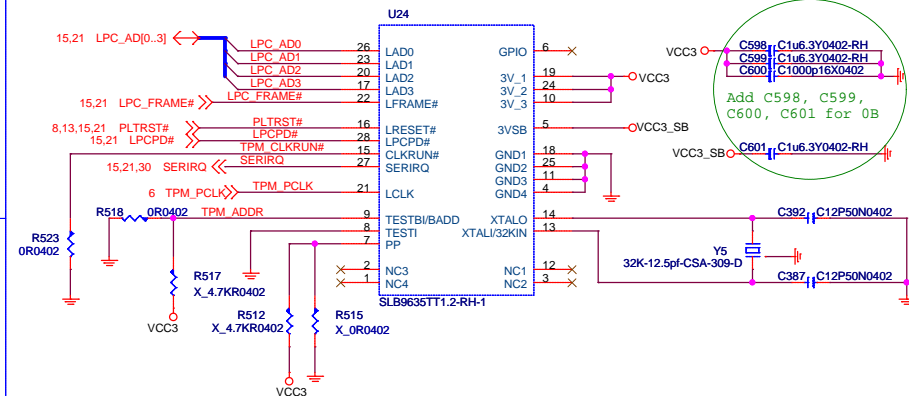
LPC Debug Port



Add J1LPC1 for 0B

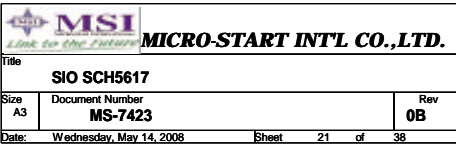
TPM 1.2

IO Address: 0x02E

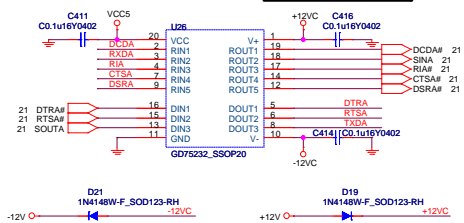


MICRO-START INT'L CO.,LTD.

Title			TPM/FAN/LPC Debug Port
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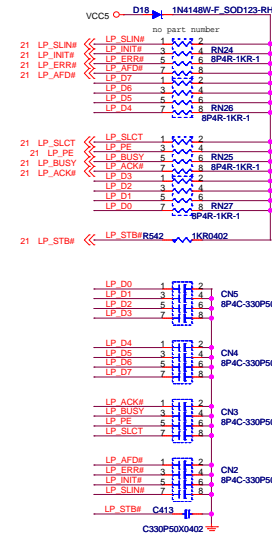
SERIAL PORT 1



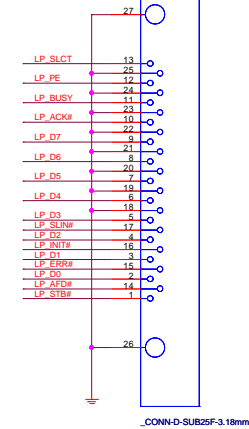
Wake On Modem Header



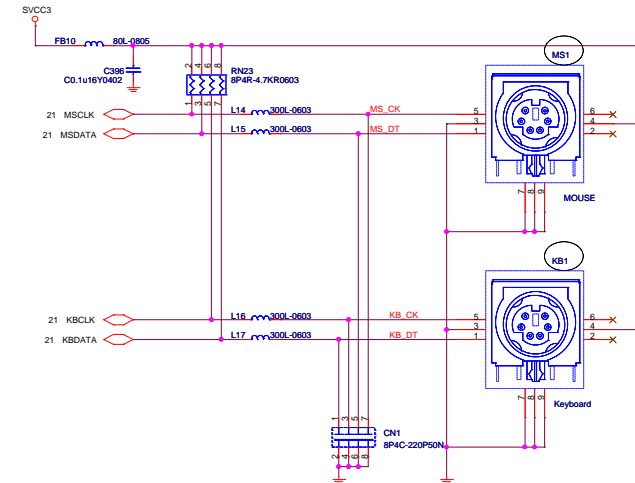
PARALLAL PORT



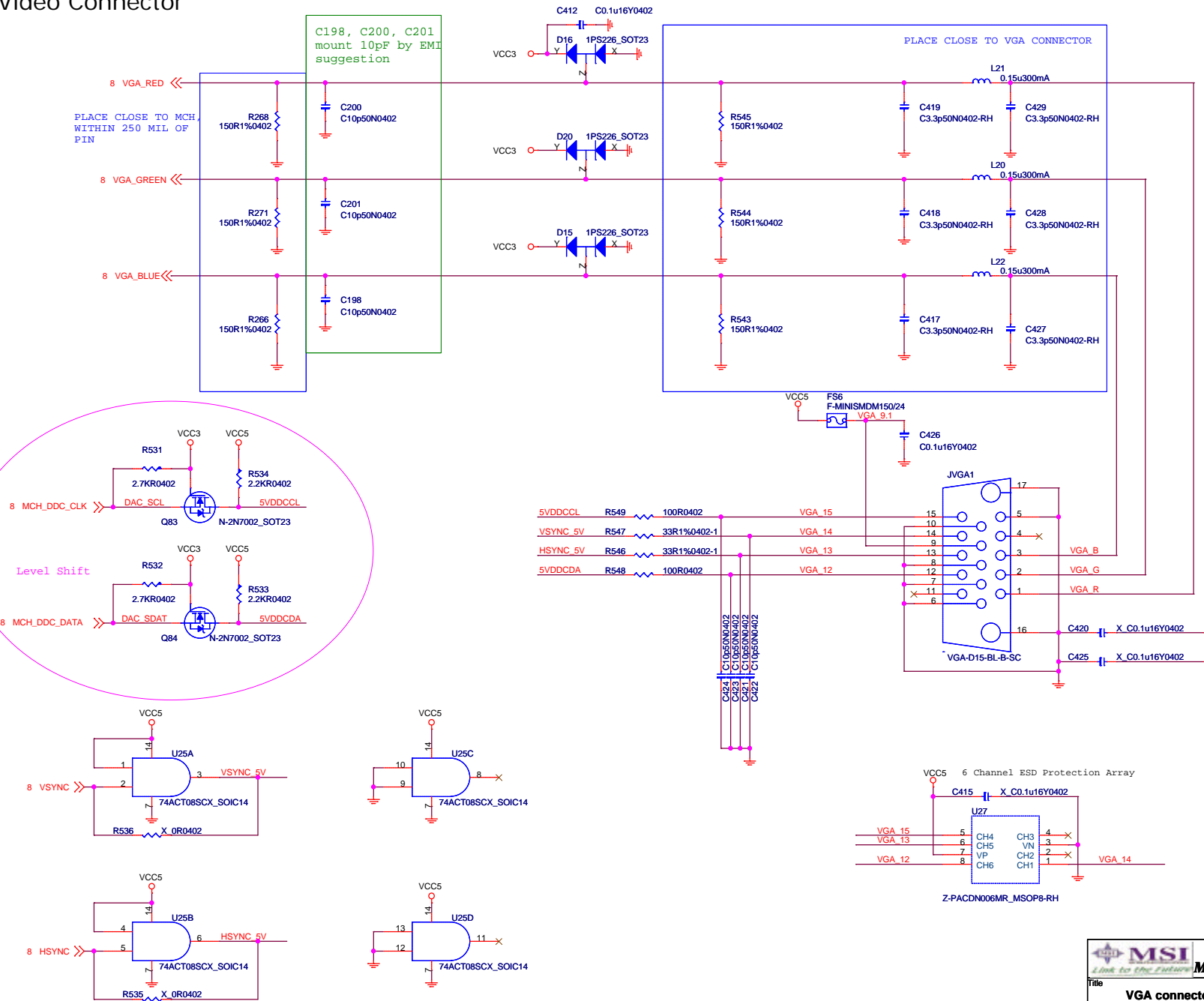
LPT1



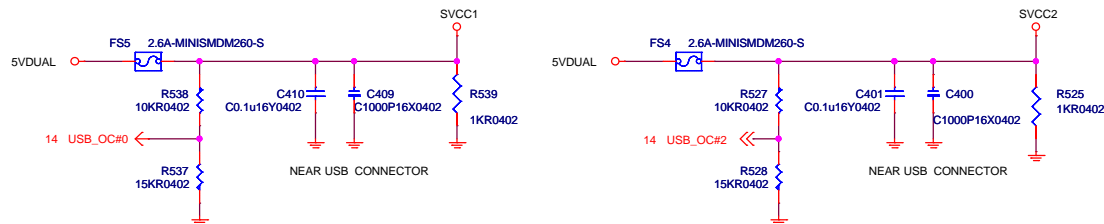
PS2 KEYBOARD & MOUSE CONNECTOR



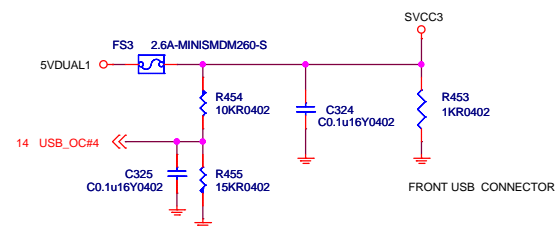
Video Connector



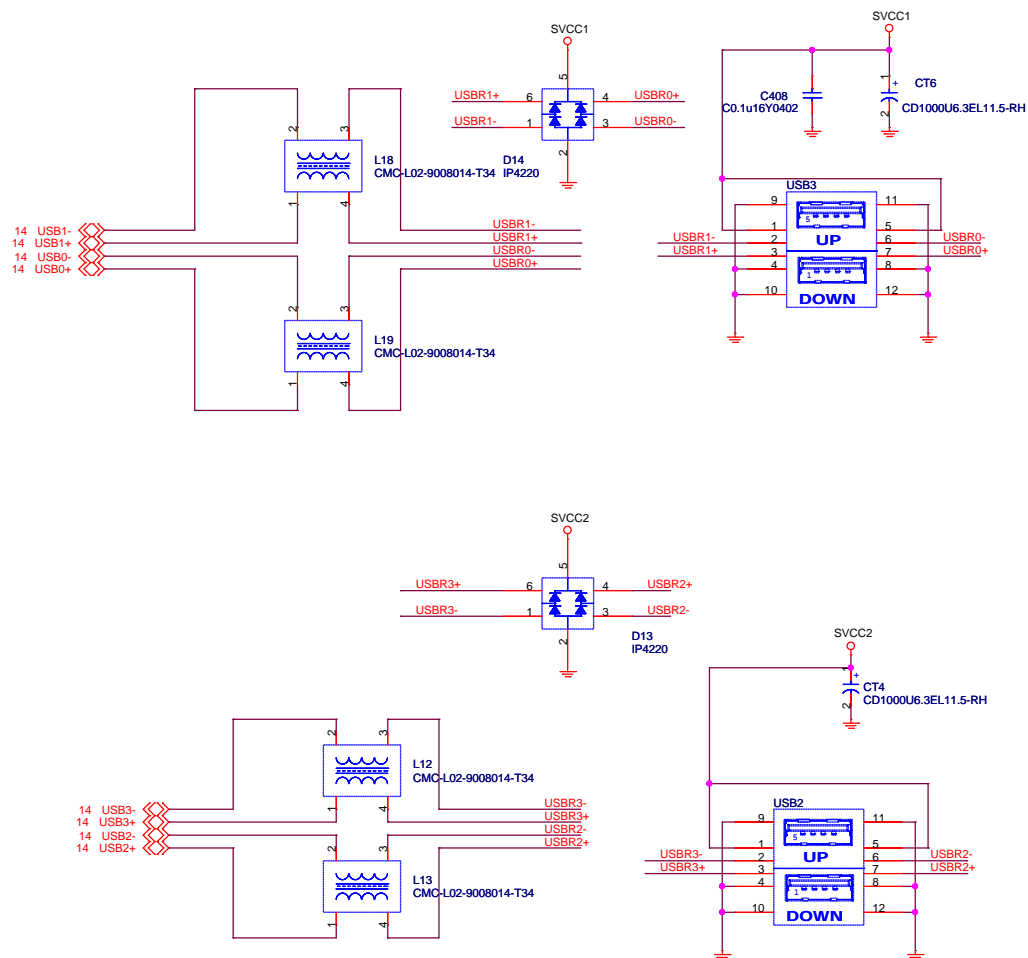
POWER CIRCUIT FOR USB PORT 0,1,2,3



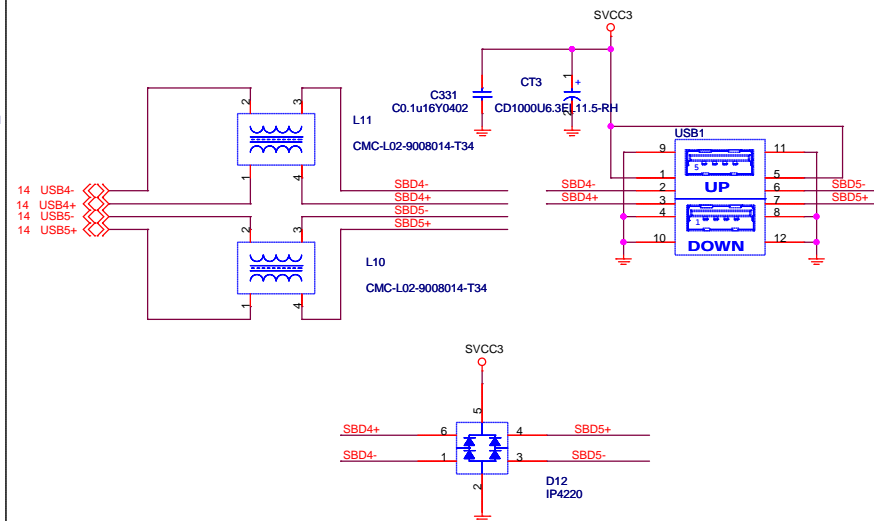
POWER CIRCUIT FOR USB PORT 4,5



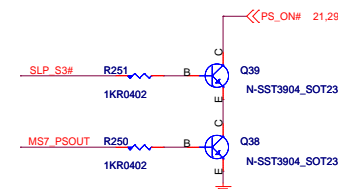
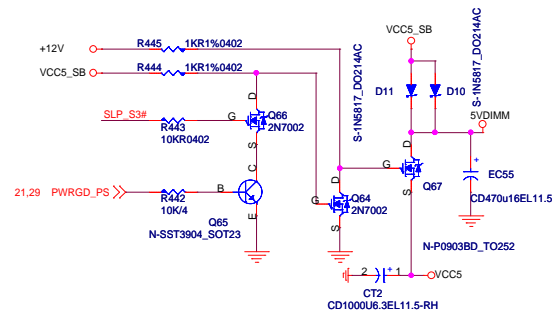
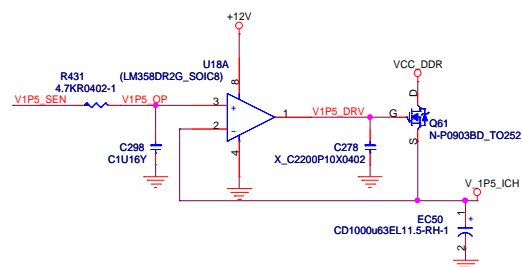
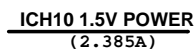
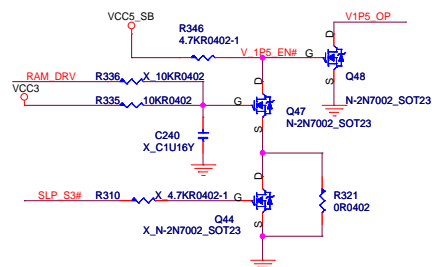
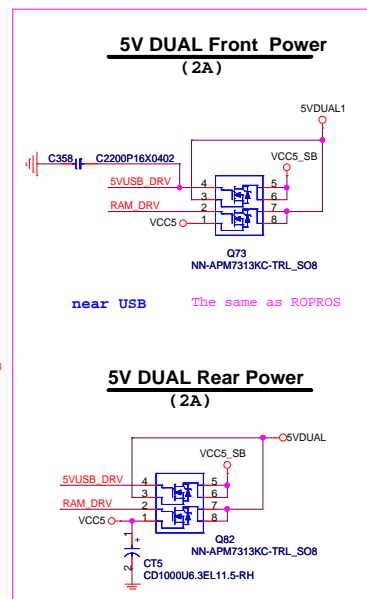
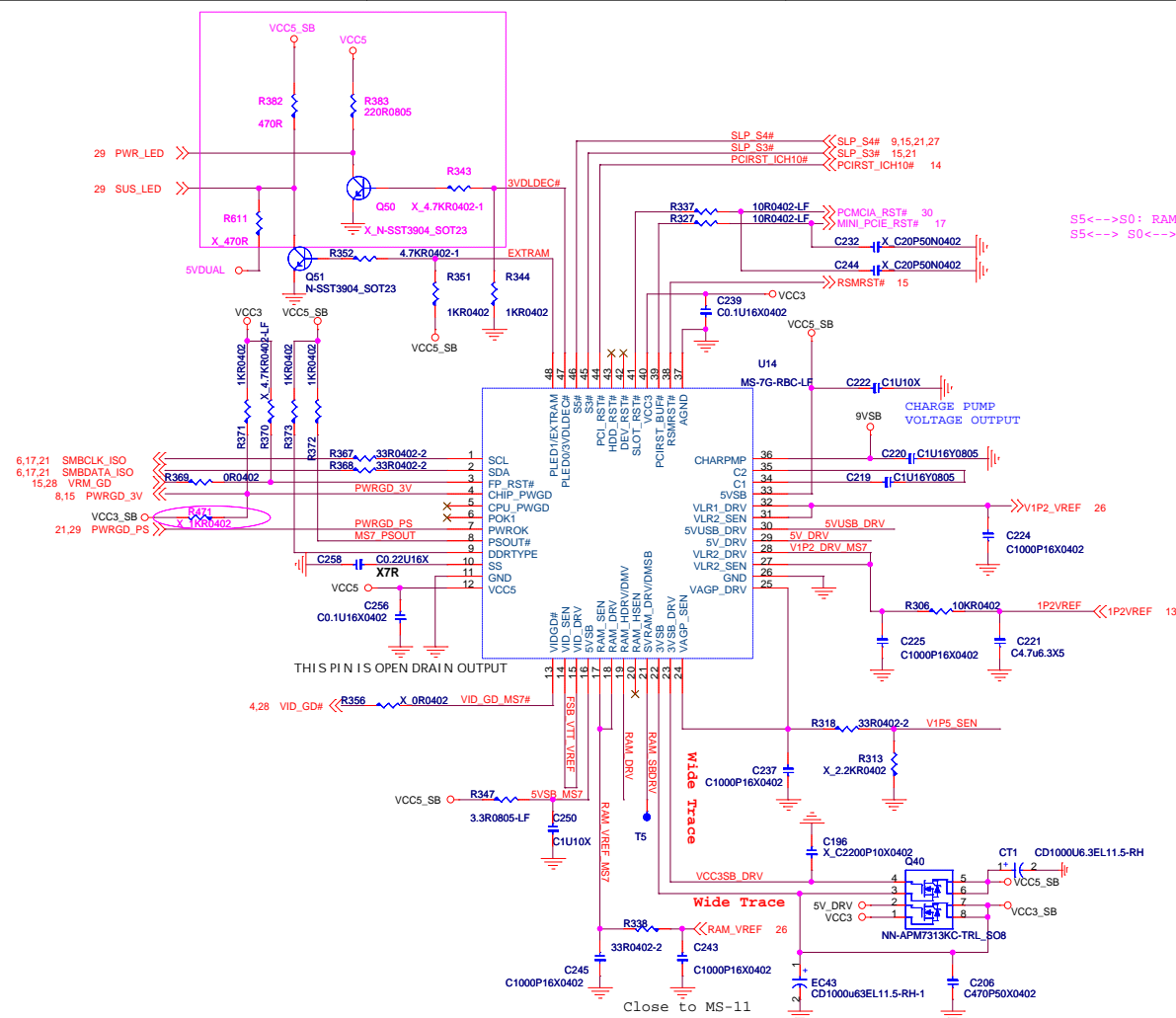
REAR PANEL USB CONNECTOR FOR USB PORT 0,1,2,3



FRONT PANEL USB CONNECTOR FOR USB PORT 4,5

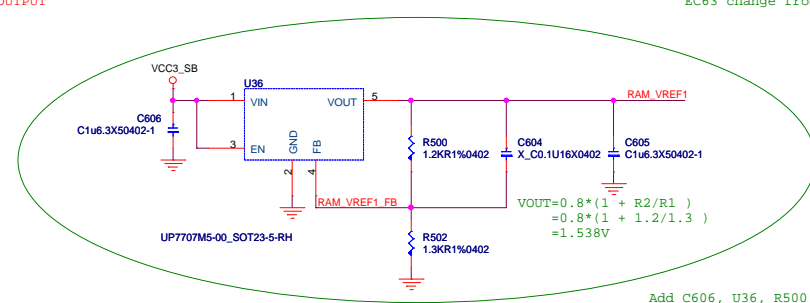


ACPI Controller

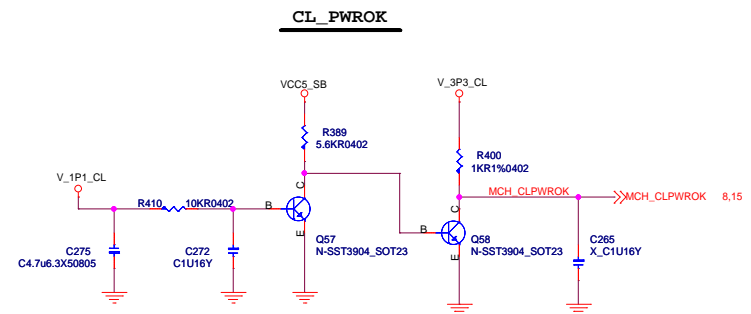
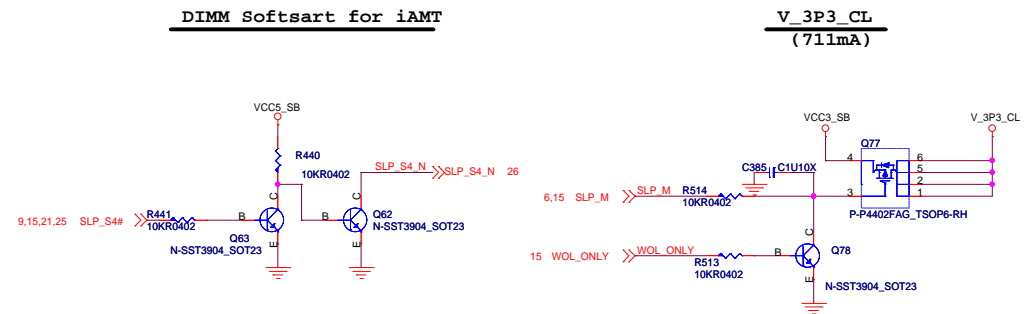



[illegible]

EC62 change from 1000uF to 820uF for 0B



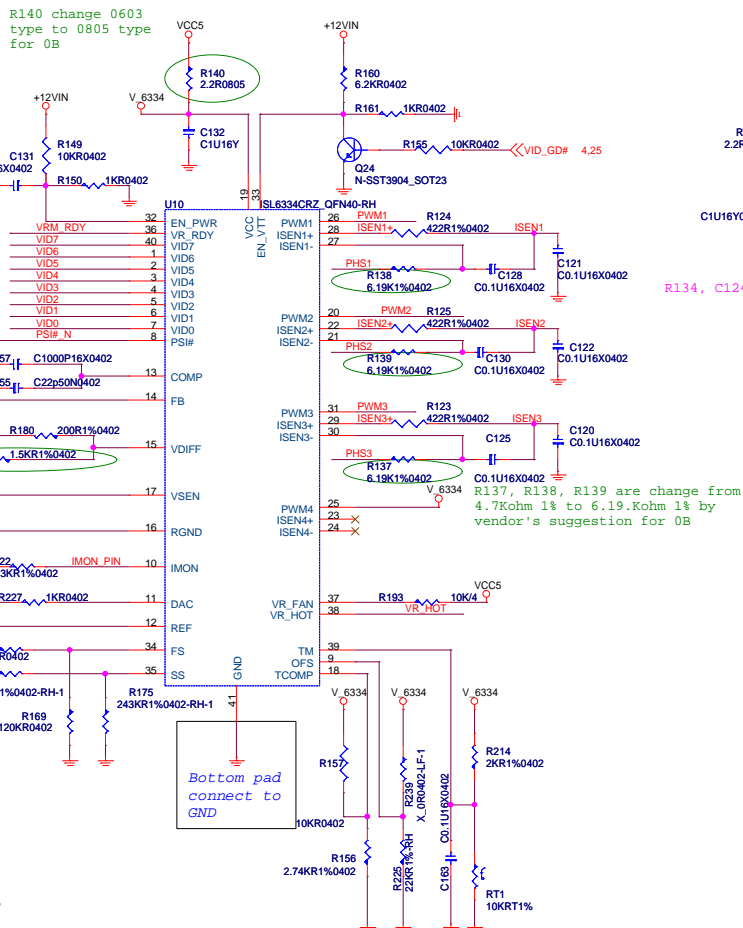
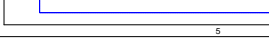
R177, R185 not mount; mount 1.1K Ω to R187; mount 12.4K Ω to R179,
reverse C603 for 0B



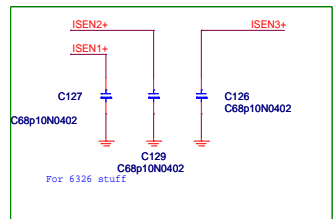
 MSI <small>Micro-Star International, Inc.</small>		MICRO-START INTL CO.,LTD.	
Title iAMTCL_POWER			
Size	Document Number MS-7423	Rev 0B	
Date: Monday, May 19, 2008		Sheet 27 of 38	

3Phases

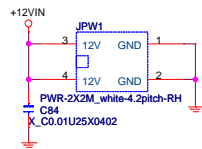
for 0B



C126, C127, C129 are changed from 100pF to 68pF by vendor's suggestion



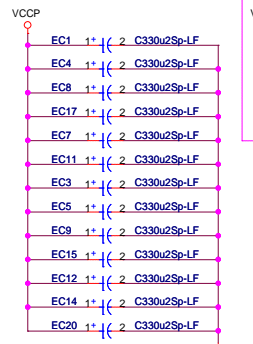
ATX12V Power Connector



TDK
NTCG104KE104ET

```
VR FAN TRIP:1.69V ~ 80 degC
VR HOT TRIP:1.44V ~ 90 degC
```

SP Capactiors



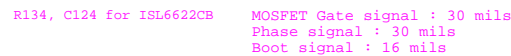
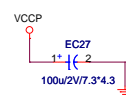
CP Solder size

EC68 1+ (2 C330u2Sp-LF

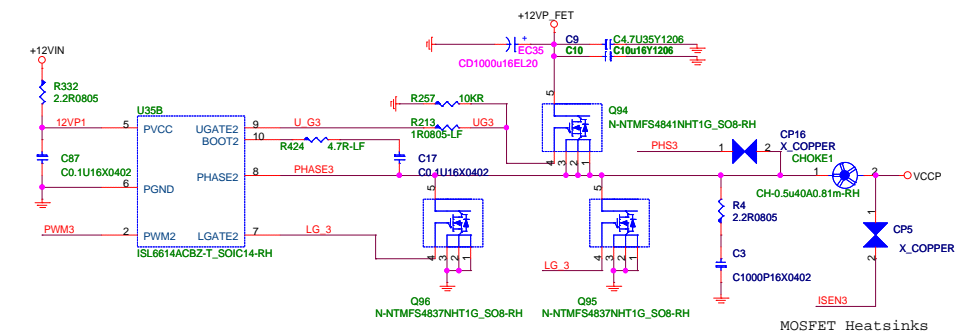
EC67 1+ (2 C330u2Sp-LF

EC66 1+ (2 C330u2Sp-LF

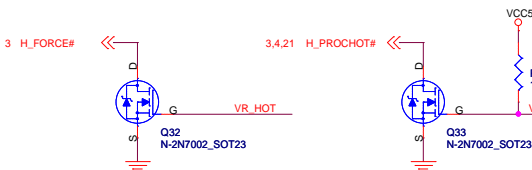
SP Capacitors




```
MOSFET Gate signal : 30 mils
Phase signal : 30 mils
Boot signal : 16 mils
```

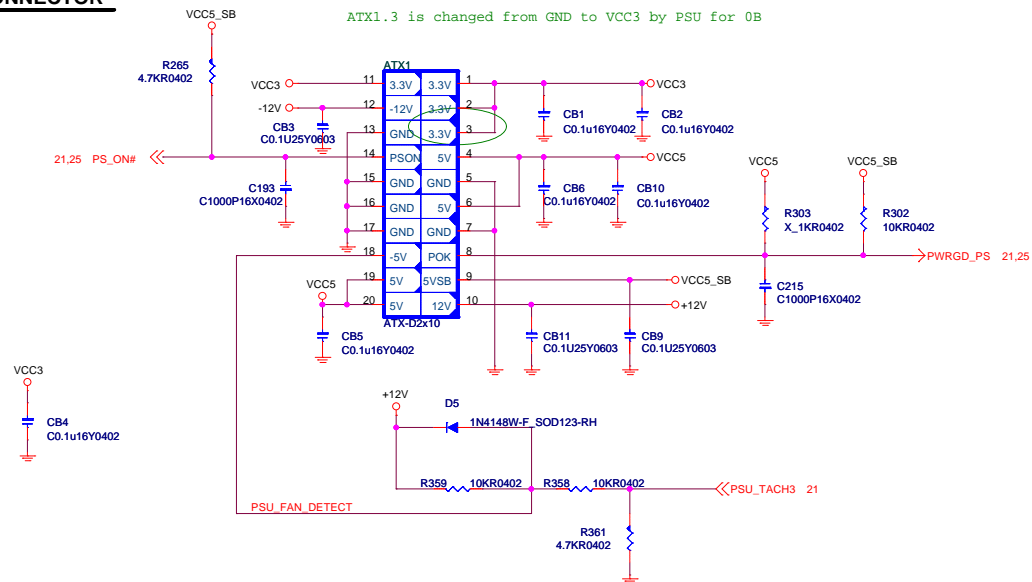


VRM solution change from DR.MOS to PowerPack for 0B



 MSI <small>Micro-Star International Co., Ltd.</small> <i>Look for the Dragon</i>	MICRO-START INT'L CO., LTD.		
Intersil 6334 3Phases			
Title	MS-7423		Rev 0B
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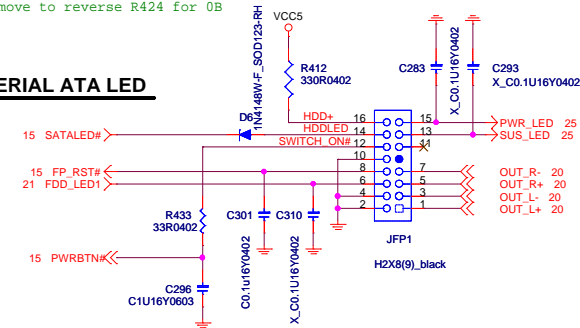
ATX CONNECTOR



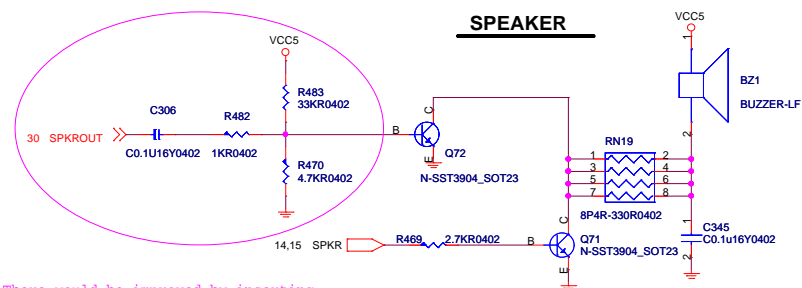
Front Panel

remove to reverse R424 for 0B

SERIAL ATA LED

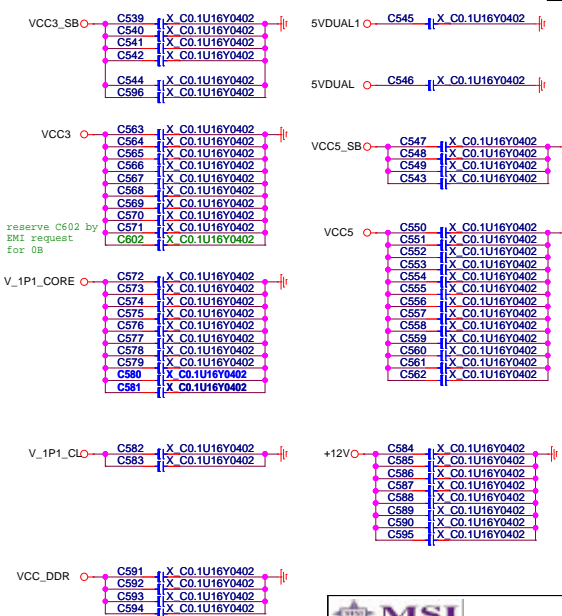


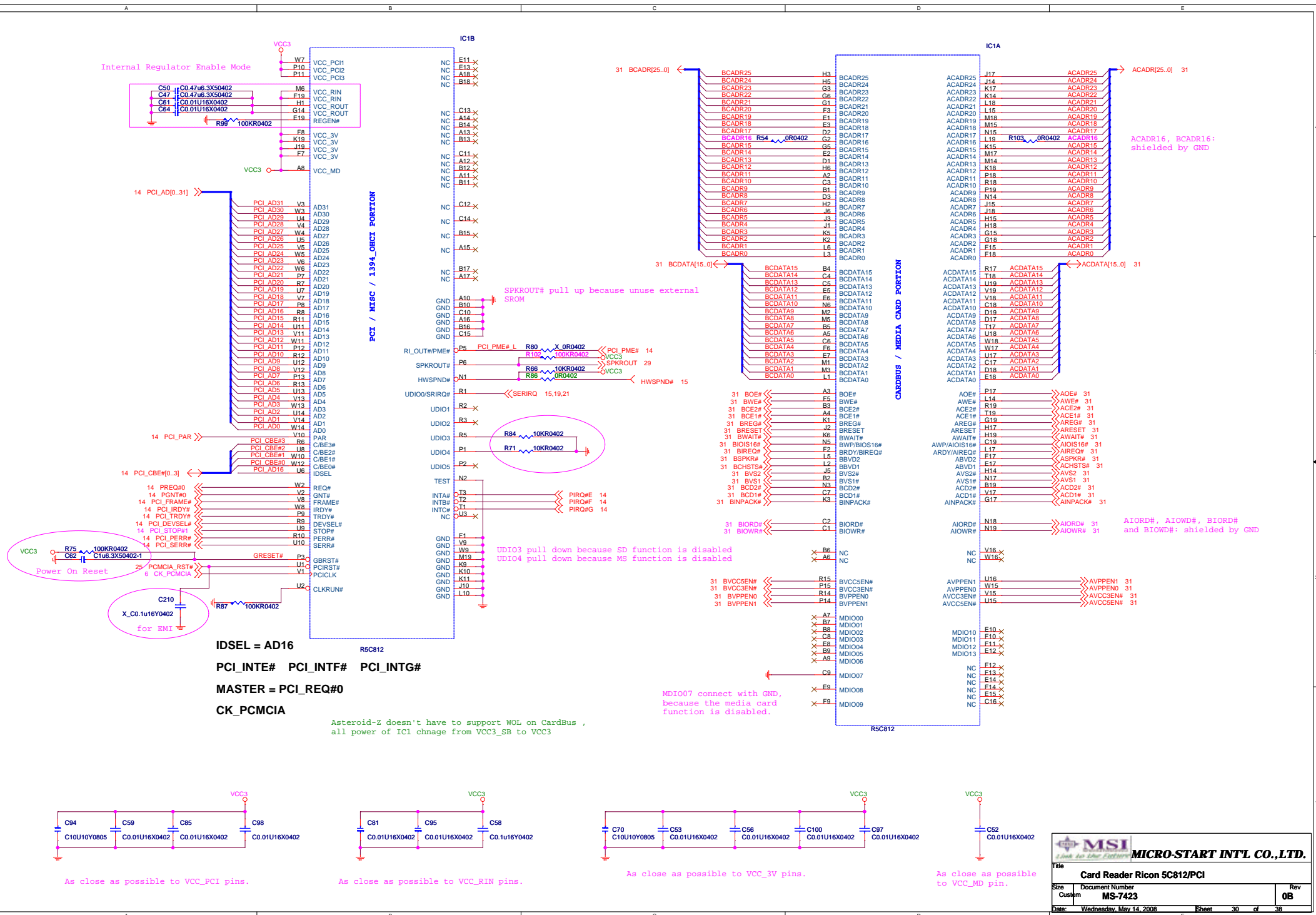
SPEAKER



There would be improved by inserting some 32bits CardBus card

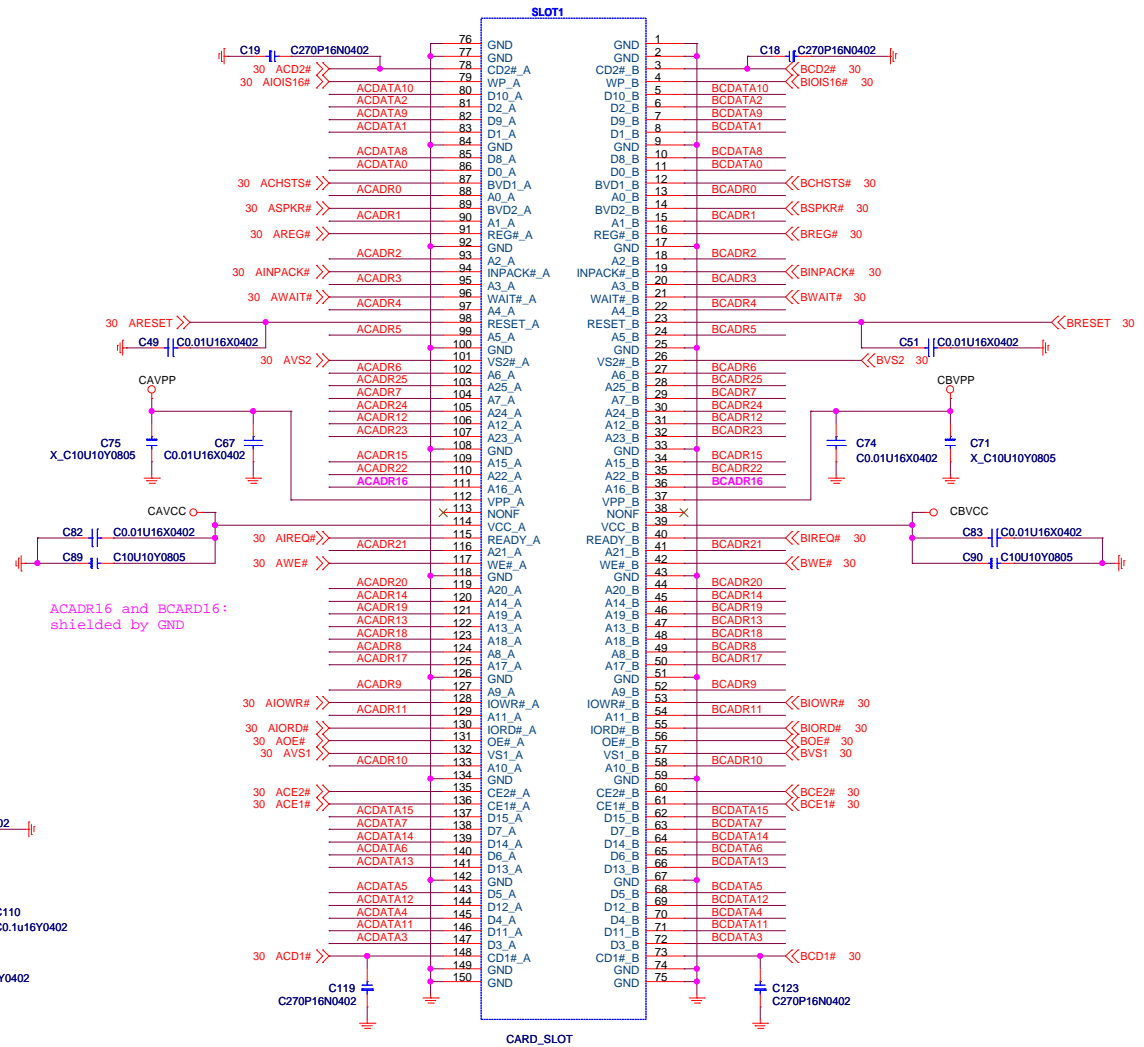
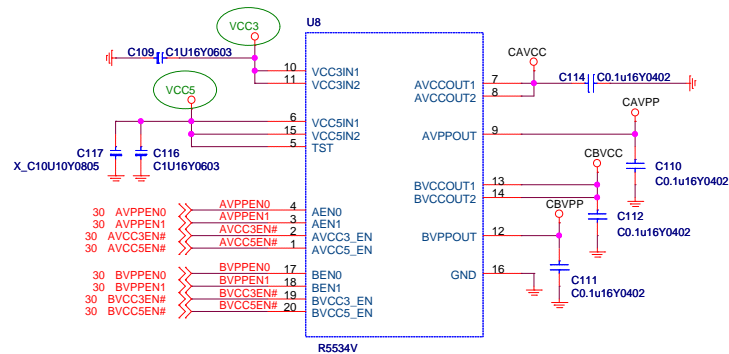
EMI decoupling cap





30 BCADR[25..0] > _____
 30 BCDA[15..0] <-> _____
 30 ACADR[25..0] > _____
 30 ACDA[15..0] <-> _____

Asteroid-Z doesn't have to support WOL on CardBus ,
 input power of U8 change from VCC3_SB& 5V_DUAL to
 VCC3 & VCC5 and remove Q25, R166, C142, Q22





Manual Parts

JBAT1(1-2)1



JMP/GREEN/A

J4(1-2)1

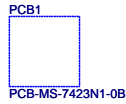


JMP/GREEN/A

JCH1(1-2)1



JMP/GREEN/A



PCB-MS-7423N1-0B



BIOS_LABEL1

LAB1



X_MODEL_LABEL

U13_HS2
H1X3[2]M_BLACK-RH-2



U13_HS3
H1X3[2]M_BLACK-RH-2

U13_HS2 & U13_HS3 change to
the same Asteriod-S3 by mechanical request on 04/16

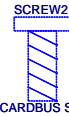
U15_HS1



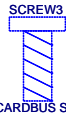
NB_HEATSINK



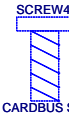
CARDBUS SCREW



CARDBUS SCREW



CARDBUS SCREW



CARDBUS SCREW

Audio Jack EMI solution



GASKET



GASKET



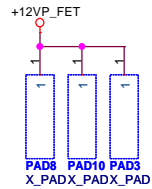
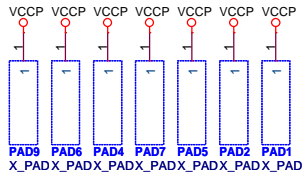
CLAMP1



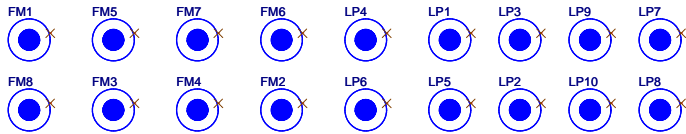
CLAMP2



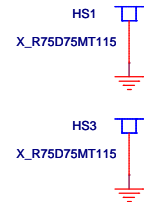
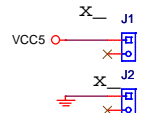
CLAMP3



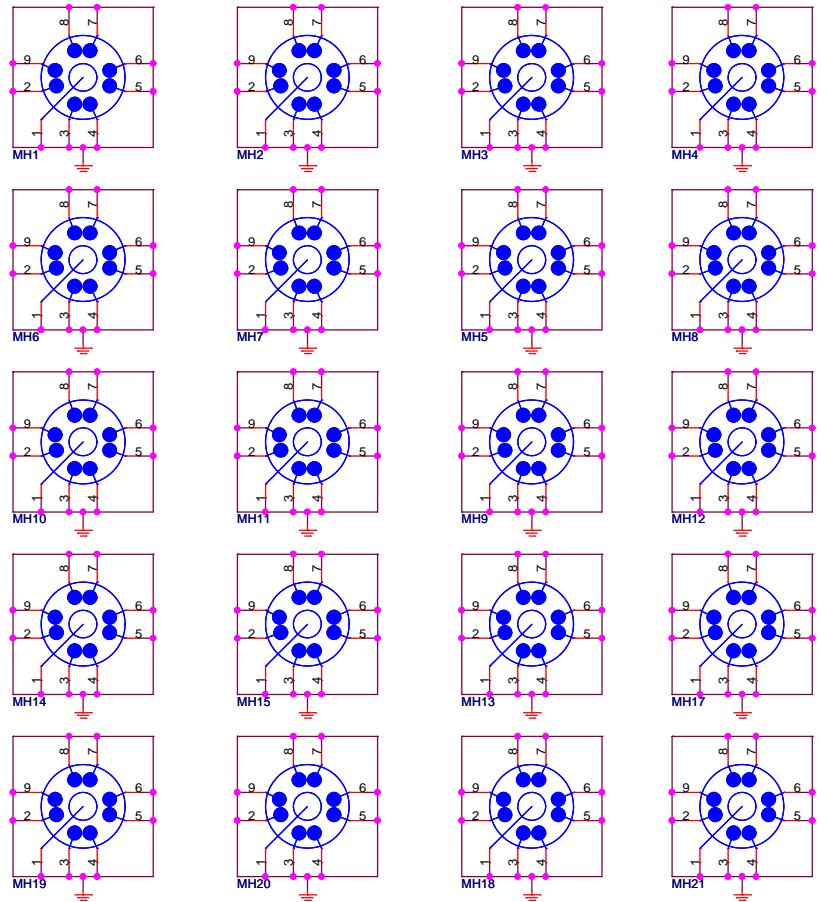
Optics Orientation Holes



Simulation

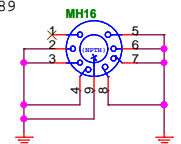



For thermal reserved



for power cable holder and FP:
HOLES315D189

added HS5 & HS6 by mechanical
request for 0B on 04/25



 MSI <i>Link the Best Partner</i>		MICRO-START INTL CO.,LTD.	
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ICH10

GPIO Pin	Type	Default	Function	Power	MUXED/ UNMUXED	Pin-out
GPIO 0	I/O	GPIO	BMBUSY# function, Pull-up to VCC3 with 10K	VCC3	MUXED	N7
GPIO 1	I/O	GPIO	Pull-up to VCC3 with 10K	VCC3	MUXED	AK21
GPIO 2	I/O	GPIO	PIRQ#E pull-up to VCC3 with 8.2K	VCC3		K6
GPIO 3	I/O	GPIO	PIRQ#F pull-up to VCC3 with 8.2K	VCC3		L7
GPIO 4	I/O	GPIO	PIRQ#G pull-up to VCC3 with 8.2K	VCC3		F2
GPIO 5	I/O	GPIO	PIRQ#H pull-up to VCC3 with 8.2K	VCC3		G2
GPIO 6	I/O	GPIO	Pull-up to VCC3 with 10K	VCC3	MUXED	AH22
GPIO 7	I/O	GPIO	Pull-up to VCC3 with 10K	VCC3	MUXED	AK23
GPIO 8	I/O	GPIO	Pull-up to VCC3_SB with 10K	VCC3_SB	UNMUXED	A20
GPIO 9	I/O	GPO/WOL	WOL_ENABLE/GPIO9, pull-down with 100K	VCC3_SB	MUXED	A18
GPIO 10	I/O	GPIO	Detect AUDIO Devices, Pull-up to VCC3_SB with 10K	VCC3_SB	MUXED	C17
GPIO 11	I/O	SMBALERT#	SMB_ALERT# pull-up to VCC3_SB with 10K	VCC3_SB		C16
GPIO 12	I/O	GPO	LAN_DISABLE connect to LAN Boazman	VCC3_SB	UNMUXED	A8
GPIO 13	I/O	GPIO	SIO_PME# connect to SIO, pull-up VCC3_SB with 10K	VCC3_SB	UNMUXED	A19
GPIO 14	I/O	GPIO	Pull-up to VCC3_SB with 10K directly	VCC3_SB	MUXED	A9
GPIO 15	I/O	GPO	PCI_STOP# connect to CLK Gen and R5C812	VCC3_SB	MUXED	C15
GPIO 16	I/O	GPO	NC	VCC3	UNMUXED	M2
GPIO 17	I/O	GPIO	Pull-up to VCC3 with 10K directly	VCC3	MUXED	AH21
GPIO 18	I/O	GPO	GTLREF GPO , Pull-up to VCC3 with 10K directly	VCC3	UNMUXED	K1
GPIO 19	I/O	GPIO	Pull-up to VCC3 with 10K	VCC3		AE20
GPIO 20	I/O	GPO	GTLREF GPO	VCC3	UNMUXED	AF5
GPIO 21	I/O	GPIO	Pull-up to VCC3 with 10K	VCC3		AK25
GPIO 22	I/O	GPIO	Pull-up to VCC3 with 10K	VCC3	MUXED	AJ24
GPIO 23	I/O	LDRQ1#	LDRQ_1# pull-up VCC3 with 10K(reserved)	VCC3	MUXED	J3
GPIO 24	I/O	GPO	NC	3.3V_SB	MUXED	A14
GPIO 25	I/O	GPO	CPU_STOP# connect to CLK Gen	3.3V_SB	UNMUXED	B18
GPIO 26	I/O	GPO	S4 STATE# pull-up to VCC3_SB with 1K ohm(reserved)	3.3V_SB		C11
GPIO 27	I/O	GPO	PANEL_DETECT pull up to VCC3 with 10Kohm	3.3V_SB		A11
GPIO 28	I/O	GPO	LCD_S1_ENA pull up to VCC3_SB with 10Kohm(reserved)	3.3V_SB		G18
GPIO 29	I/O	OC5#	OC#4 connect to USB connector	3.3V_SB		N1
GPIO 30	I/O	OC6#	OC#4 connect to USB connector	3.3V_SB		N5
GPIO 31	I/O	OC7#	OC#4 connect to USB connector	3.3V_SB		M1
GPIO 32	I/O	GPO	NC	VCC3	UNMUXED	K2
GPIO 33	I/O	GPO	Pull-up to VCC3 with 4.7K through JCI1 jumper.(Default)	VCC3	UNMUXED	AF6
GPIO 34	I/O	GPO	GPIO34 connect to HWSPND# directly	VCC3	UNMUXED	AH5
GPIO 35	I/O	GPO	GP35 pull-up to VCC3_SB with 10Kohm(reserved)	VCC3		L1
GPIO 36	I/O	GPIO	Pull-up to VCC3 with 10K directly	VCC3		AE21
GPIO 37	I/O	GPIO	Pull-up to VCC3 with 10K directly	VCC3		AE22
GPIO 38	I/O	GPIO	Pull-up to VCC3 with 10K directly	VCC3		AK24
GPIO 39	I/O	GPIO	Pull-up to VCC3 with 10K directly	VCC3		AH23
GPIO 40	I/O	OC1#	OC#0 connect to USB connector	3.3V_SB		N3
GPIO 41	I/O	OC2#	OC#2 connect to USB connector	3.3V_SB		P7
GPIO 42	I/O	OC3#	OC#2 connect to USB connector	3.3V_SB		R7
GPIO 43	I/O	OC4#	OC#4 connect to USB connector	3.3V_SB		N2
GPIO 44/45	I/O	OC8/9#	OC#4 connect to USB connector	3.3V_SB		P3/R6
GPIO 46/47	I/O	OC10/11#	OC#4 connect to USB connector	3.3V_SB		T7/P1
GPIO 48	I/O	GPIO	pull-up VCC3 with 10K	VCC3		AD20
GPIO 49	I/O	GPO	DMI strapping , pull-down 2.2K(reserved) to GND	VCC3		AJ25
GPIO 50	I/O	REQ1#	REQ1 pull-up to VCC5 with 2.7K	VCC5	MUXED	G13
GPIO 51	I/O	GNT1#	GNT1#(Unused)	VCC3	MUXED	A7
GPIO 52	I/O	REQ2#	REQ2 pull-up to VCC3 with 8.2K	VCC5	MUXED	F13
GPIO 53	I/O	GNT2#	GNT2#(Unused), pull-down 1K ohm(reserved) to GND	VCC3	MUXED	C7
GPIO 54	I/O	REQ3#	REQ3 pull-up to VCC5 with 2.7K	VCC5	MUXED	G8
GPIO 55	I/O	GNT3#	GNT3#(Unused), pull-up 1K ohm(reserved) to VCC3	VCC3	MUXED	F7
GPIO 56	I/O	GPIO	Clear password, pull-up to VCC3_SB with 10K.	3.3V_SB	MUXED	F16
GPIO 57	I/O	GPIO	Pull-up to V_3P3_CL with 1K	3.3V_SB	MUXED	C12
GPIO 58	I/O	SPI_CS1	SPI_CS#(Not Use) , SPI_CS1_F#(Not Use)	3.3V_SB	MUXED	F23
GPIO 59	I/O	OC0#	OC#0 connect to USB connector	3.3V_SB		P5
GPIO 60	I/O	LINKALERT	LINKALERT# pull-up to VCC3_SB with 10K	3.3V_SB		F18
GPIO 61	I/O		LPCPD# pull-up to VCC3_SB with 10Kohm(reserved)	3.3V_SB		R1
GPIO 62	I/O		NC	3.3V_SB		R5
GPIO 72	I/O		BATTLOW# pull-up to VCC3_SB with 10K ohm	3.3V_SB		C13

SIO - SMSC-5617C Configuration

PIN NAME	PIN#	USAGE	Input/Output
GP41	77	SIO_PME#	OUTPUT
GP25	30	SMBCLK	INPUT
GP26	29	SMBCLK_ISO	INPUT
GP35	28	SMBDATA	OUTPUT
GP42	27	SMBDATA_ISO	OUTPUT

PCI Configuration

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
Ricoh R5C812	PIRQ#E PIRQ#F PIRQ#G	PREQ#0 PGNT#0	AD16	CK_PCMCIA

PCI_RST# DISTRIBUTION

SOURCE	PCIRST#	LOAD
ICH10	PCMCIA_RST#	Ricoh R5C812
	PCIRST_ICH10#	MS7
MS7	MINI_PCIE_RST#	MINI PCIE
	PLTRST#	TPM
	RSMRST#	ICH10
NB	H_CPUURST#	CPU

DDR III DIMM Config.


DEVICE	ADDRESS	CLOCK
DIMM 1	A0H	SCLK_A0/SCLK_A0#
		SCLK_A2/SCLK_A2#
DIMM 2	A4H	SCLK_B0/SCLK_B0#
		SCLK_B2/SCLK_B2#

Jumper Setting

JBAT1	(1-2)Normal	(2-3)Clear CMOS
JCI1	(1-2)Normal	(2-3)ME Disable for FPROG
J4	(1-2)short: Normal	(1-2)Open: Clear PW

SMBus Distribution

SMBus	Power	Load
SMBCLK	VCC3_SB	SIO, ICH10, MINI PCI EXPRESS
SMBCLK_ISO	VCC3	DIMM, CLK GEN, MS7

 MICRO-START INT'L CO., LTD.	
Title GPIO MAP	
Size	Document Number
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LGA775-CPU		
0.8375V - 1.6000V Core	-	84A
1.1V FSB Vtt	-	4.6A

Eaglelake (GMCH)		
1.1V FSB_VTT	-	1.2 A
1.1V Core TBD (USE LB)	-	13.8A
1.1V DMI/PCI Exp.	-	2.47 A
1.5V VCC_DDR	-	3.33A
1.5V VCC_SMCLK	-	350mA
3.3V VCCA_DAC	-	66 mA
3.3V VCC33	-	15.8mA
1.1V Vcc CL	-	4.3A

ICH10		
1.1V DMI	-	41 mA
1.1V Core	-	1.16A
1.5V_A USB/SATA/PLL	-	1.652A
1.5V_B PCI Exp.	-	0.646A
VCCRTC	-	6 uA
3.3V CL	-	19 mA
1.5V GbE LAN	-	87 mA
3.3V VccSus3_3	-	200mA
3.3V Vcc3_3	-	308mA
3.3V 10/100 LAN	-	19 mA
3.3V GbE LAN	-	1 mA
3.3V HDA	-	32 mA
3.3V SusHDA	-	33 mA

HD Audio ALC262VD		
3.3V AUDIO	-	40mA
5V AUDIO	-	200mA

IDTCV184-2		
3.3V VDD_48/PCI/REF	-	250mA
0.3V-1V CPU/SRC/DOT/PLL	-	80mA

Boazman GbE		
3.3V_SB I/O & LED	-	15.5mA
1.8V AVDD	-	418.2mA
1.0V Core	-	277.2mA

ISL6334		
VCCP VRD11.1	-	0.8375V-1.6000V
3-Phase Switch	-	

W83310DS		
VTT_DDR	-	0.75V Linear 0.83A

MS11+ SW-Power		
VCC_DDR	-	1.5V PWM 13.86A

MS11+ SW-Power		
V_1P1_CORE	-	1.1V PWM 23.27A

MS7 Controller		
V_1P1_CL	-	1.1V Linear 3A

MS7 Controller		
V_1P5_ICH	-	1.5V Linear 2.385A
VCC3_SB	-	3.3V Linear 3.96A
5VDUAL1	-	5V Switch 4.367A
5VDIMM	-	5V Switch 8.29A

DDRIII x2 & TERMINATOR		
0.75V VTT_DDR	-	1.2A
1.5V VCC_DDR (S0,S1)	-	3.6A
1.5V VCC_DDR (S3)	-	TBDmA

LVDS		
5V	-	340mA
+3.3V	-	375mA
+3.3V	-	20mA

Mini PCI_E x1 slot		
+3.3Vaux	-	1100mA
+3.3V	-	375mA

PCMCIA dual slot		
+5VSB	-	1A
+3.3Vaux	-	375mA

USB x 6		
+5V (S0,S1)	-	3A
+5V (S3)	-	20mA

PS2		
+5V (S0,S1)	-	345mA
+5V (S3)	-	2.0mA


5VAudio		
+5VR	-	500mA

3V
Battery

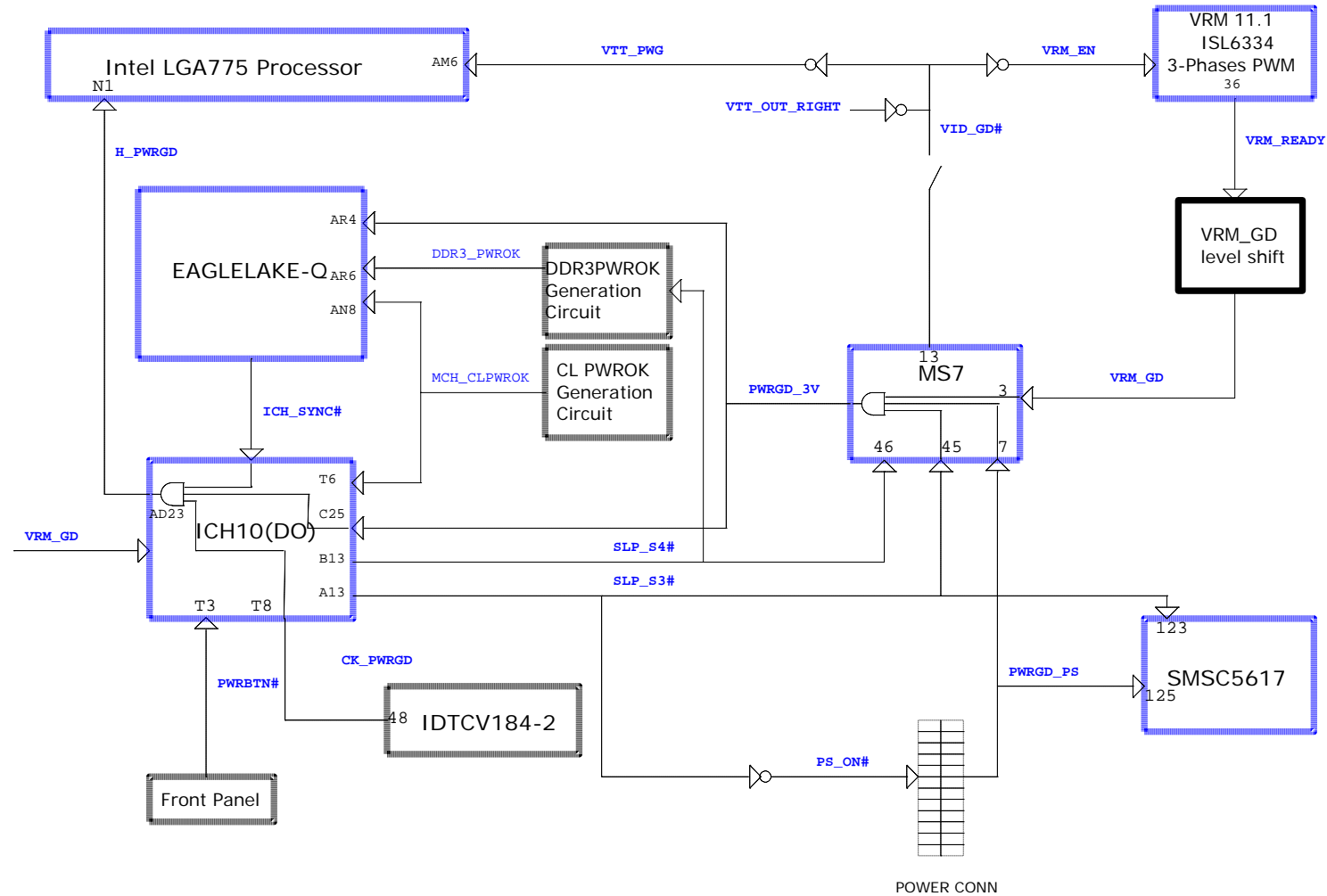
+12V		
ATX	-	2x2

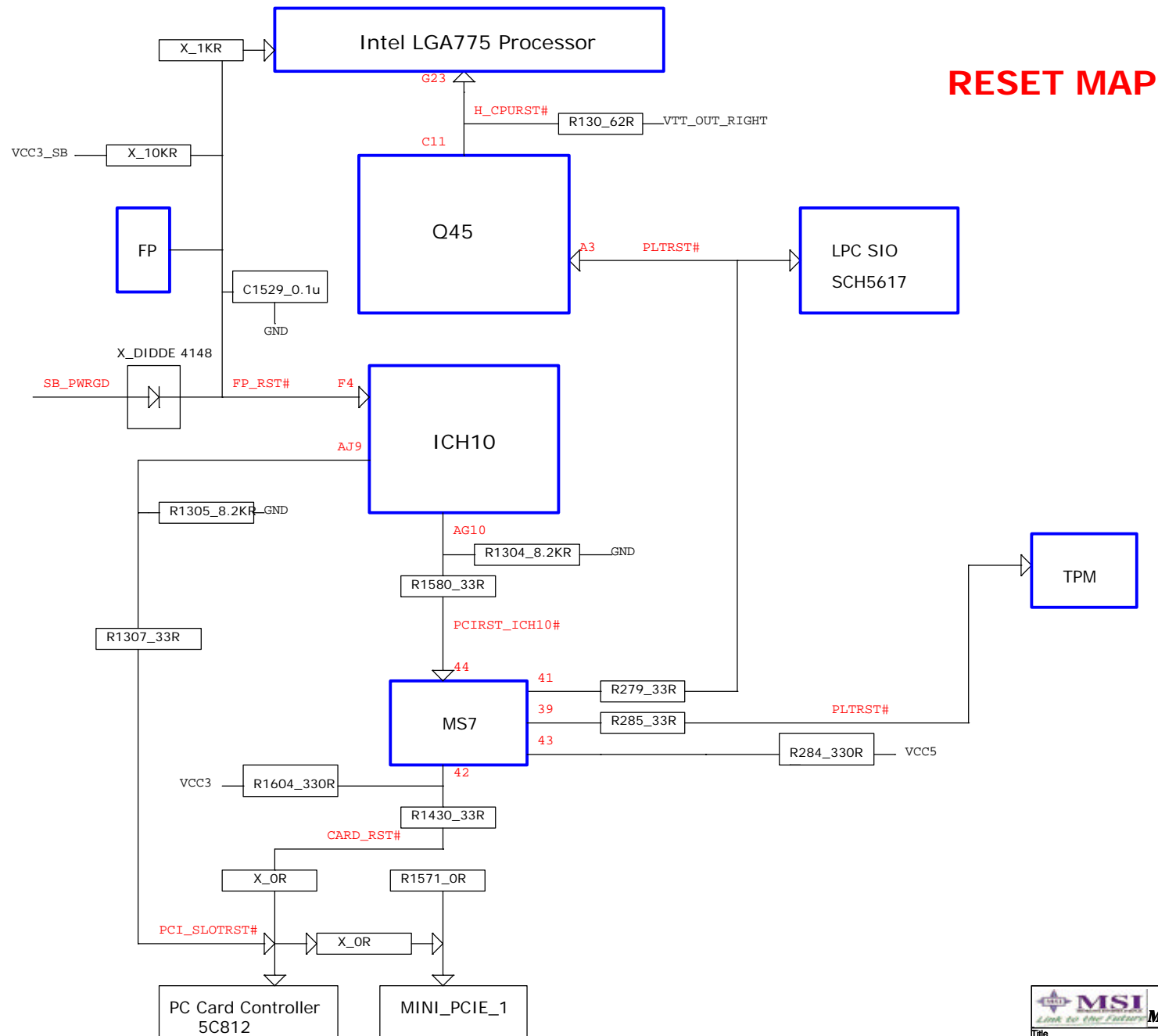
+5V (10A)	+3.3V (12A)	+5VSB (10A)	+12V (12A)
ATX POWER			

PSU: DPS-200PB-168 A REV:50F

 MICRO-START INTL CO.,LTD.	
Title	POWER MAP
Size	Document Number
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PWROK MAP





0A

(1) Remove the AC Coupling Capacitor(C306,C307) on Rx signal line. Because these Capacitor were mounted on Rxsignal line in MINI Card module board from NECP comment on page 17 on 2/20

0B

(1) Remove R152 and PM_DPRSTR_N(net) connect directly to U7.T2 on page 3

(2) R109, R111 not mount because they have unused on page 3

(3) U7.A23, U7.B23, U7.C23 change to test point on page 4

(4) Remove L1, R100, C87, C80, C92(they have unused), add Q92, R612, R613(add level shift between PROCHOT# and ICH10 (GPIO32) for NECP economy mode) on page 4

(5) Remove Q34, Q36, add Q91(unify the materials) on page 4

(6) C28, C29 are changed from 27pF to 47pF on page 6

(7) EC60 change from 1000uF to 820uF and EC58 mount 820uF on page 8

(8) R158 no mount, Q27 mount, remove R142, add Q34 (Intel PSI# design update)on page 8

(9) Remove Q54, Q56, add Q36, R385 mount(Intel suggestion), C262 change from 1uF to 12nF(Intel suggestion) on page 9

(10) C287 change from Y5V to X7R, C290 change from 0603 type/Y5V to 0402 type/X7R (follow Intel design)on page 9

(11) Remove R257 and L7 change from 10uH to 0ohm on page 10

(12) C44, C45 change from 27pF to 33pF on page 13

(13) Support Danbury, R390 mount 10Kohm on page 14

(14) Remove R409(it has unused), R332(immediately); R308 mount 33ohm(use ICH10 DRAMPWROK function pin); add GPIO_32(net); R242, R245not mount (Intel suggestion) , R398 not mount(GPIO18 is already output function, don't need to pull-up); reserve C307(RC timing) on page 15

(15) C403, C404, C405 mount 0.1uF on page 18

(16) Added the four decoupling capacitors(C598, C599, C600, C601) should be placed as short as possible to the respective 3Vand 3VSB pins of the chip on page 19

(17) Add LPC debug port at JLPCL on page 19

(18) Solving the audio become to mute, rename to AC_RST# (net) on page 20

(19) C528 is changed to T34(vendor) by buyer request on page 20

(20) Remove R500, R502(because they have unused), add D25(Due to Peci_REQUEST have leakage, SMSC have workaround to add a diode to avoid)on page 21

(21) remove R492(immediately) and C367 change from 270pF to 220pF(the same as LE) on page 21

(22) Remove C224 on page 25

(23) EC62, EC63 change from 1000uF to 820uF ; EC61 mount 820uF; R437 & R439 not mount; Add C606, U36, R500, R502, C605, reverse C604; R177, R185 not mount; mount 1.1K Ω to R187; mount 12.4K Ω to R179, reverse C603; CHOKE6, CHOK5, COIL1, COIL2 change for transient and noise on page 26

(25) VRM solution change from DR.MOS to PowerPack(the same as LE), pls refer to page 28

(26) U13_HS2 & U13_HS3 are changed to the same AZ-S3 by mechanical request on 04/16

(27) R607, R608 are change from 6.8Kohm Ω to 18Kohm Ω , R572, R581 are change from 20Kohm Ω to 13Kohm Ω by customer request on page 20 on 04/17

(28) R140 change 0603 type to 0805 type(unify the materials) ; R137, R138, R139 are change from 4.7Kohm Ω to 6.19.Kohm Ω ; C126, C127, C129 are changed from 100pF to 68pF ; R191 is changed form 1.91K ohm Ω to 1.5K ohm Ω by vendor's suggestion on page 28

(29) U15 stepping change from A1 to A3 on page 7~11

(30) U13_HS2 & U13_HS3 change to the same Asteriod-S3 by mechanical request on 04/16

(31) Asteroid-Z doesn't have to support WOL on CardBus , all power of ICL chnage from VCC3_SB to VCC3 , remove Q25, R166, C142, Q22 from NECP comment on page 30 & 31 on 04/18

(32) ATX1.3 is changed from GND to VCC3 by PSU , remove to reverse R424 for 0B on page 29

(33) C189&C190 change from Y5V to X7R on page 14

(34) C381&C383 change from Y5V to X7R on page 18

(35) U30, U32 are changed from SCHMITT-TRIGGER to BUFFER and are added R615, R614, R616 by customer request on page 20 on 4/22

(36) R387 and R388 not mount on page 9

(37) remove R404(reserved) on page 15

(38) remove to reserve R100 and R166 from CH7308B's datasheet rev2.1 on page 13

(39) C198, C200, C201 are mounted 1pF by EMI suggestion on page 23

(40) reserved decoupling cap to C602 by EMI request on page 29

(41) added HS5 & HS6 by mechanical request on page 32 on 04/25

(42) Add EC70 near CPU on page 26

(43) U13 stepping change to B0 on page 14 ~ 16

(44) EC2, EC6, EC10, EC13, EC18 are changed to a height of 11mm by mechanical & thermal request on page 13

(45) reserved C607,C608, C609, C610 by checklist request on page 21

(46) add FS7 by checklist request on page 13


(47) R3, Q1, Q2, R5, Q3 not mount because pin 27 of LCD_1 is NC and BIOS no support S1 mode on page 13

D

C

B

A

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(48) R601 and R606 are change from 47ohm 5% to 51ohm 1% by customer request on page 20 on 05/14

(49) R298, R350 not mount (pin 27 of LCD_1 is NC pin) and R350 not mount(BIOS no support S1 mode) on page 15

(50) R456, C326, R457, R451, R452 not mount on page 27

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